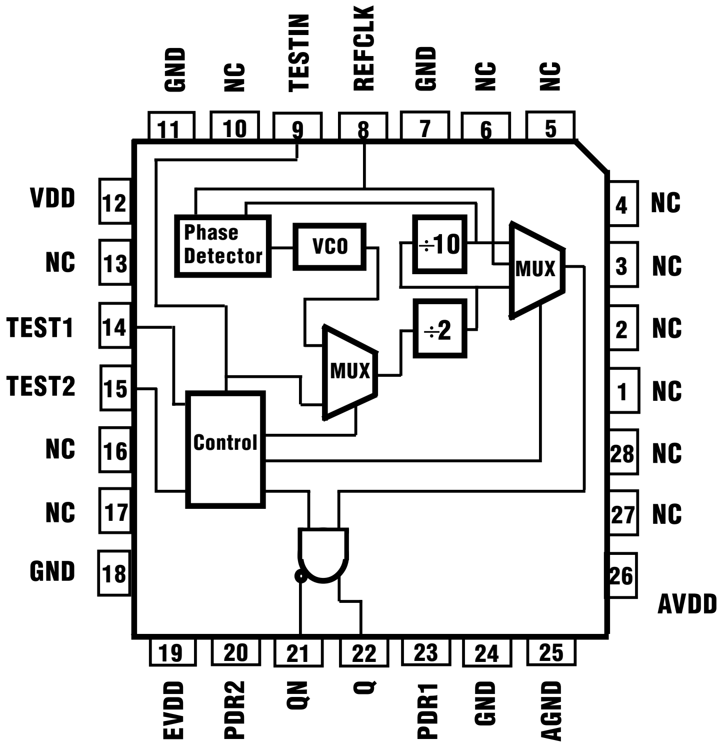
TRIQUINT TQS SEMICONDUCTOR, INC.

TQ2059

High-Frequency Clock Generator

Figure 1. Pinout Diagram


GND
NC
TESTIN
REFCLK
GND
NC
NC
11
10
9
8
7
6
5
VDD 12
NC 13
TEST1 14
TEST2 15
NC 16
NC 17
GND 18
4 NC
3 NC
2 NC
1 NC
28 NC
27 NC
26 AVDD
Phase Detector
VCO
÷10
÷2
MUX
MUX
Control
19
20
21
22
23
24
25
EVDD
PDR2
QN
Q
PDR1
GND
AGND

TriQuint's TQ2059 is a high-frequency clock generator. It utilizes a 20 MHz to 35 MHz TTL input to generate a 200 MHz to 350 MHz PECL output. The TQ2059 has a completely self-contained Phase-Locked Loop (PLL) running at 400 MHz to 700 MHz. This stable PLL allows for a low period-to-period output jitter of 120 ps (max), and enables tight duty-cycle control of 55%to 45% (worst case).

The TQ2059 provides optional 200-ohm on-chip pull-down resistors which are useful if the output is AC-coupled to the device being driven. In order to use these resistors, pin 20 (PDR2) should be connected to pin 21 (QN), and pin 23 (PDR1) should be connected to pin 22 (Q).

Various test modes on the chip simplify debug and testing of systems by slowing the clock output or by bypassing the PLL.

Features

- *Output frequency range: 200 MHz to 350 MHz*
- *One differential PECL output: 600 mV (min) swing*
- *Common-mode voltage:*
  V_{DD} –1.2 V (max),
  V_{DD} –1.6 V (min)
- *Period-to-period output jitter:*
  30 ps peak-to-peak (typ)
  120 ps peak-to-peak (max)
- *Reference clock input: 20 MHz to 35 MHz TTL-level crystal oscillator*
- *Self-contained loop filter*
- *Optional 200-ohm pull-down resistors for AC-coupled outputs*
- *+5 V power supply*
- *28-pin J-lead surface-mount package*
- *Ideal for designs based on DEC Alpha AXP™ processors*

Figure 2. Simplified Block Diagram

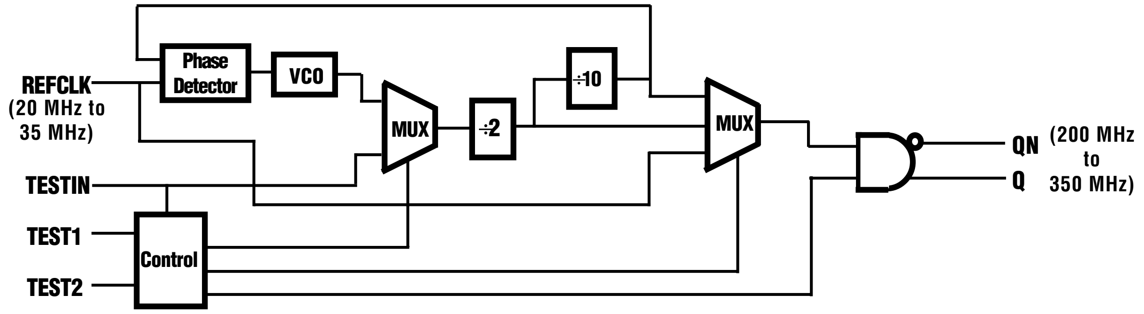

Phase Detector
VCO
MUX
÷2
÷10
MUX
REFCLK
(20 MHz to 35 MHz)
TESTIN
TEST1
TEST2
Control
QN
Q
(200 MHz to 350 MHz)

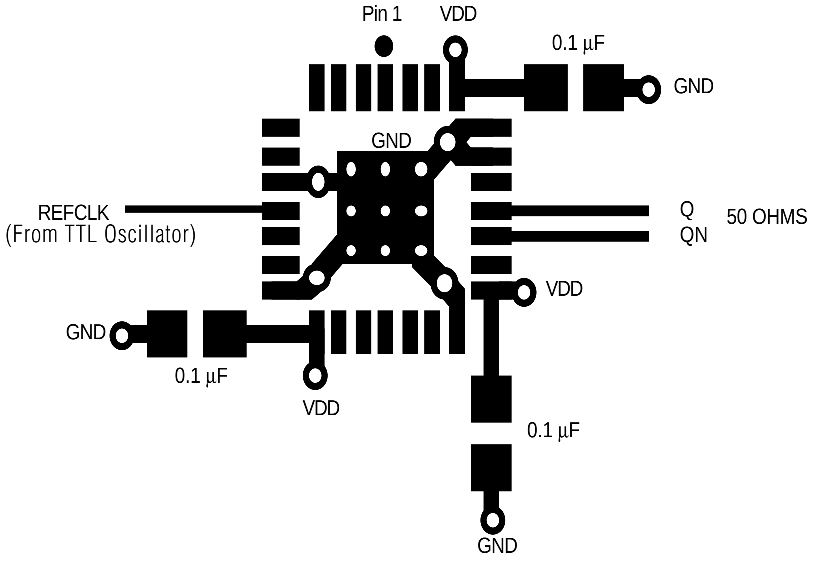
Table 1. Mode Selection

Mode	*TEST1*	*TEST2*	*TESTIN*[1]	*REFCLK*[2]	*Q, QN*
1 (Test)	0	0	$f_{TESTCLK}$	“don't care”	$f_{TESTCLK} \div 20$
2 (Test)	0	1	“don't care”	“don't care”	0, 1
3 (Test)	1	0	$f_{TESTCLK}$	“don't care”	$f_{TESTCLK} \div 2$
4 (Bypass)	1	1	0	f_{REFCLK}	f_{REFCLK}
5 (Normal)	1	1	1	f_{REFCLK}	10 x f_{REFCLK}[3]

Note: 1. In modes 1 and 3, TESTIN may be used to bypass the PLL. A clock input at TESTIN will be divided as shown.
2. REFCLK = 20 MHz to 35 MHz.
3. Q, QN = 200 MHz to 350 MHz.

Recommended Layout

(Not to scale)


Pin 1
VDD
0.1 µF
GND
GND
REFCLK
(From TTL Oscillator)
Q
QN
50 OHMS
VDD
GND
0.1 µF
VDD
0.1 µF
GND

Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient temperature with power applied	–55°C to +110°C
Supply voltage to ground potential	–0.5 V to +7.0 V
DC input voltage	–0.5 V to (V_{DD} + 0.5) V
DC input current	–30 mA to +5 mA
Package thermal resistance (MQuad)	θ_{JA} = 45°C/W
Die junction temperature	T_J = 150°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. The device should be operated only under the DC and AC conditions shown below.

DC Characteristics (V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C)[1]

				Limits [1]		
Symbol	**Description**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH voltage	V_{CC} = Min PECL load	V_{CC}–1.20		V_{CC}–0.50	V
V_{OL}	Output LOW voltage	V_{CC} = Min PECL load	V_{CC}–2.00		V_{CC}–1.60	V
V_{CMO}	Output common mode voltage	PECL	V_{CC}–1.60		V_{CC}–1.20	V
ΔV_{OUT}	Output differential voltage	PECL	0.6		1.2	V
$V_{IH}{}^2$	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
$V_{IL}{}^2$	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I_{IL}	Input LOW current	V_{DD} = Max V_{IN} = 0.40 V		–150	–400	µA
I_{IH}	Input HIGH current	V_{DD} = Max V_{IN} = 2.7 V		0	25	µA
I_I	Input HIGH current	V_{DD} = Max V_{IN} = 5.3 V		2	1000	µA
$I_{DDS}{}^3$	Power supply current	V_{DD} = Max		85	120	mA
V_I	Input clamp voltage	V_{DD} = Min I_{IN} = –18 mA		–0.70	–1.2	V

Capacitance

Symbol	**Description**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
C_{IN}	Input Capacitance	V_{IN} = 2.0 V at f = 1 MHz		6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V at f = 1 MHz		9		pF

Notes: 1. Typical limits are at V_{DD} = 5.0 V and T_A = 25˚C.
2. These are absolute values with respect to device ground and include all overshoots due to system or tester noise.
3. This parameter is measured with device not switching and unloaded.

AC Characteristics (V_{DD} = +5 V ± 5%, T_A = 0 °C to +70 °C)

Symbol	*Input Clock (REFCLK)*	*Test Conditions*	*Min*	*Typ*	*Max*	*Unit*
t_{CPWH}	CLK pulse width HIGH	Figure 2	4	—	—	ns
t_{CPWL}	CLK pulse width LOW	Figure 2	4	—	—	ns
t_{IR}	Input rise time (0.8 V – 2.0 V)		—	—	2.0	ns

Symbol	*Input Clock (REFCLK)*	*Test Conditions*	*Min*	*Typ*	*Max*	*Unit*
t_{OR}, t_{OF}	Rise/fall time (20% – 80%)	Figure 2	100	220	350	ps
t_{CYC}	Duty-cycle	Figure 2	45	50	55	%
t_{JP}^2	Period-to-Period Jitter		—	30	120	ps
t_{SYNC}^3	Synchronization Time		—	10	500	µs

Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).
2. Jitter specification is peak to peak. Period-to-Period jitter is the jitter on the output with respect to the output's previous crossing.
3. t_{SYNC} is the time required for the PLL to synchronize and assumes the presence of a CLK signal.

Figure 1

PECL Test Load

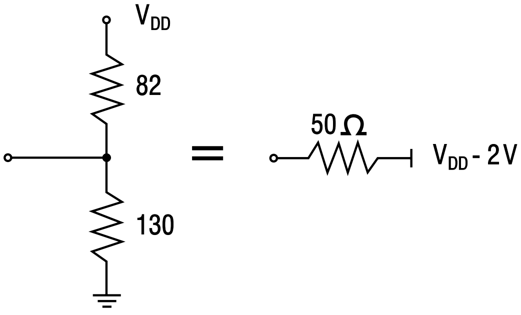
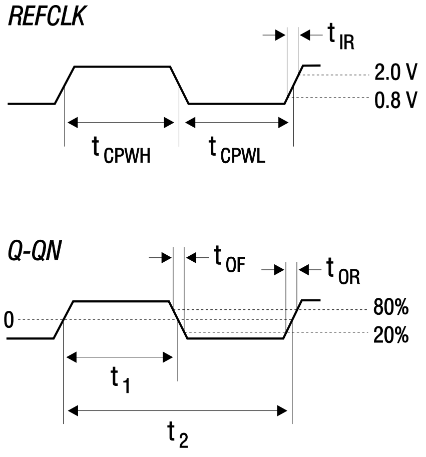


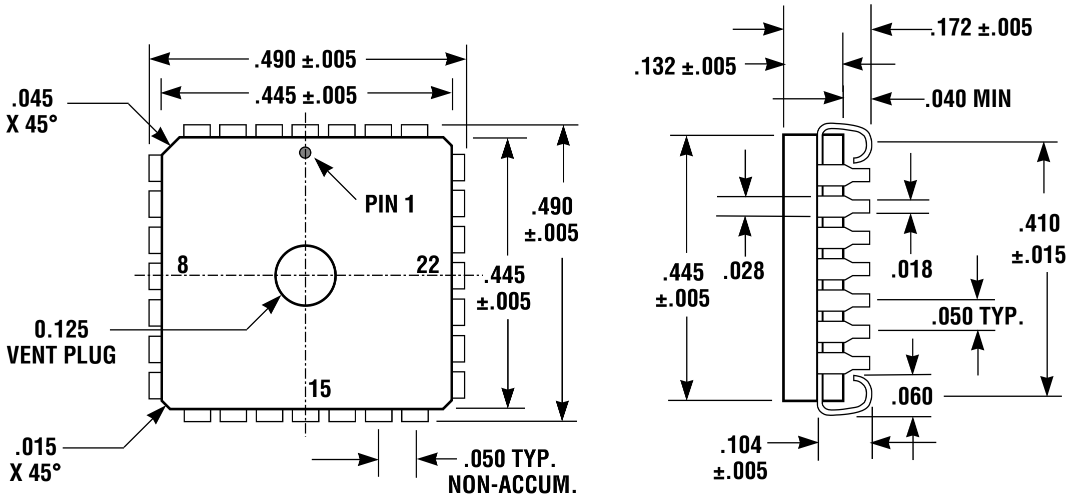
Figure 2



$$\frac{t_1}{t_2} \text{ X } 100 = 55\% \text{ to } 45\%$$

28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions in inches)


.490 ±.005
.445 ±.005
.045
X 45°
PIN 1
.490
±.005
8
22
.445
±.005
0.125
VENT PLUG
15
.015
X 45°
.050 TYP.
NON-ACCUM.
.172 ±.005
.132 ±.005
.040 MIN
.410
±.015
.445
±.005
.028
.018
.050 TYP.
.060
.104
±.005

28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	NC	No Connect	—
2	NC	No Connect	—
3	NC	No Connect	—
4	NC	No Connect	—
5	NC	No Connect	—
6	NC	No Connect	—
7	GND	Ground	—
8	REFCLK	Reference Clock	I
9	TESTIN	Test Input	I
10	NC	No Connect	—
11	GND	Logic Ground	—
12	VDD	Logic VDD (+5 V)	—
13	NC	No Connect	—
14	TEST1	Test Control 1	I
15	TEST2	Test Control 2	I
16	NC	No Connect	—
17	NC	No Connect	O
18	GND	Ground	—
19	EVDD	VDD for ECL Output (+5 V)	—
20	PDR2	Pull-down Resistor 2 (200 Ω)	I
21	QN	Differential PECL Output (–)	O
22	Q	Differential PECL Output (+)	O
23	PDR1	Pull-down Resistor 1 (200 Ω)	I
24	GND	Ground	—
25	AGND	Analog Ground	—
26	AVDD	Analog VDD (+5 V)	—
27	NC	No Connect	—
28	NC	No Connect	—

Ordering Information

To order, please specify as shown below:

TQ2059-MC *High-Frequency Clock Generator*

Temperature range: 0°C to 70°C (Commercial)

Package: 28-Pin MQuad

Additional Information

For latest specifications, additional product information,
worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**
Email: sales@tqs.com **Fax: (503) 615-8900**

For technical questions and additional information on specific applications:

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