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SEMICONDUCTOR TECHNICAL DATA

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Designer's™ Data Sheet

SWITCHMODE™ Schottky Power Rectifier

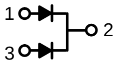
D3PAK Power Surface Mount Package

MBRV7030CTL

Motorola Preferred Device

SCHOTTKY BARRIER
RECTIFIER
70 AMPERES
30 VOLTS

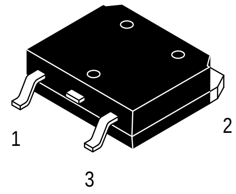
Employing the Schottky Barrier principle in a large area metal–to–silicon power rectifier. Features epitaxial construction with oxide passivation and metal overlay contact. Ideally suited for low voltage, high frequency switching power supplies; free wheeling diodes and polarity protection diodes.



- Compact Package Ideal for Automated Handling
- Short Heat Sink Tab Manufactured — Not Sheared
- Highly Stable Oxide Passivated Junction
- Guardring for Over–voltage Protection
- Low Forward Voltage Drop
- Monolithic Dual Die Construction. May be Paralleled for High Current Output.

Mechanical Characteristics:

- Case: Epoxy, Molded
- Weight: 2 Grams (approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Maximum Temperature of 260°C for 10 Seconds for Soldering
- Shipped 29 Units per Plastic Tube
- Marking: MBRV7030CTL



CASE 433A–01, Style 1
D3PAK

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage		V_{RRM} V_{RWM} V_R	30	V
Average Rectified Forward Current (At Rated V_R, T_C = 135°C)	Per Leg Per Package	I_O	35 70	A
Peak Repetitive Forward Current (At Rated V_R, Square Wave, 20 kHz, T_C = 135°C)	Per Leg	I_{FRM}	70	A
Non–Repetitive Peak Surge Current (Surge applied at rated load conditions, halfwave, single phase, 60 Hz)	Per Package	I_{FSM}	500	A
Storage / Operating Case Temperature		T_{stg}, T_C	– 55 to 150	°C
Operating Junction Temperature		T_J	– 55 to 150	°C
Voltage Rate of Change (Rated V_R, T_J = 25°C)		dv/dt	10,000	V/µs

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Case Thermal Resistance — Junction–to–Ambient (2)	Per Leg Per Leg	$R_{\theta JC}$ $R_{\theta JA}$	0.59 54	°C/W

ELECTRICAL CHARACTERISTICS

Maximum Instantaneous Forward Voltage (1), see Figure 2 (I_F = 35 A, T_J = 25°C) (I_F = 70 A, T_J = 25°C) (I_F = 35 A, T_J = 100°C)	Per Leg	V_F	 0.50 0.62 0.47	V
Maximum Instantaneous Reverse Current, see Figure 4 (Rated V_R, T_J = 25°C) (Rated V_R, T_J = 100°C)	Per Leg	I_R	 2.0 40	mA

(1) Pulse Test: Pulse Width ≤ 250 µs, Duty Cycle ≤ 2%
(2) Rating applies when using minimum pad size, FR4 PC Board

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

TYPICAL ELECTRICAL CHARACTERISTICS

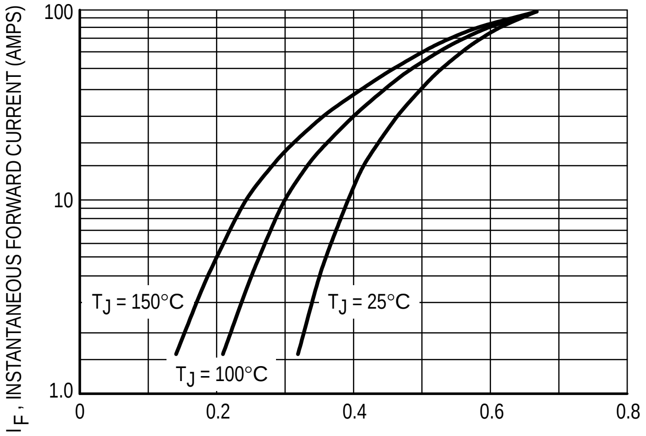


Figure 1. Typical Forward Voltage

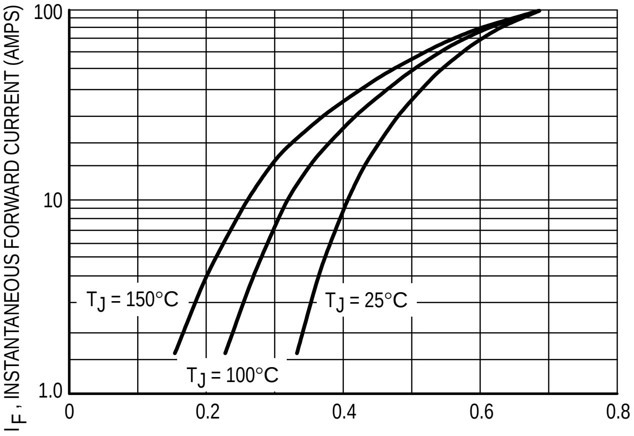


Figure 2. Maximum Forward Voltage

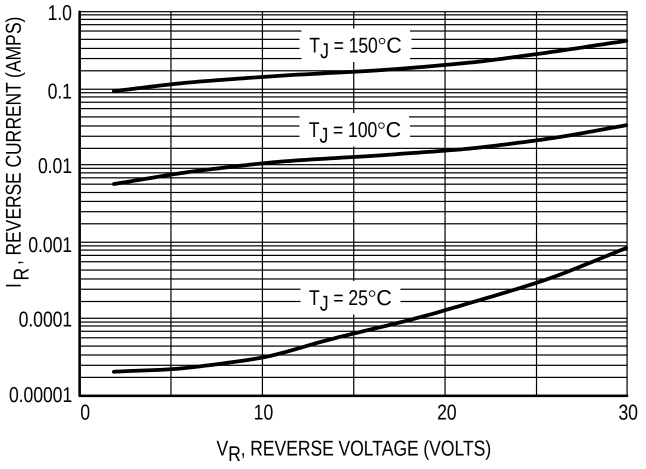


Figure 3. Typical Reverse Current

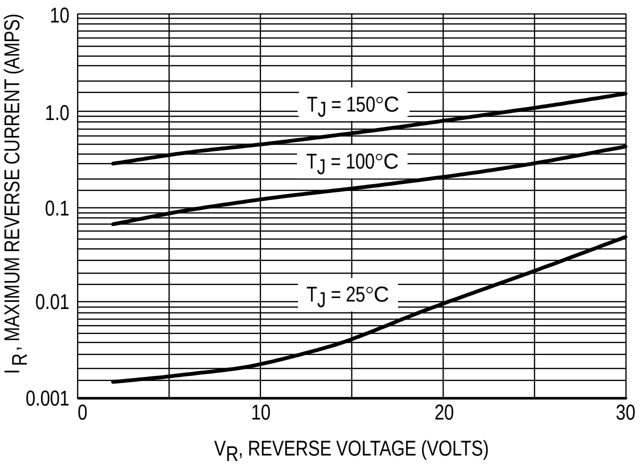


Figure 4. Maximum Reverse Current

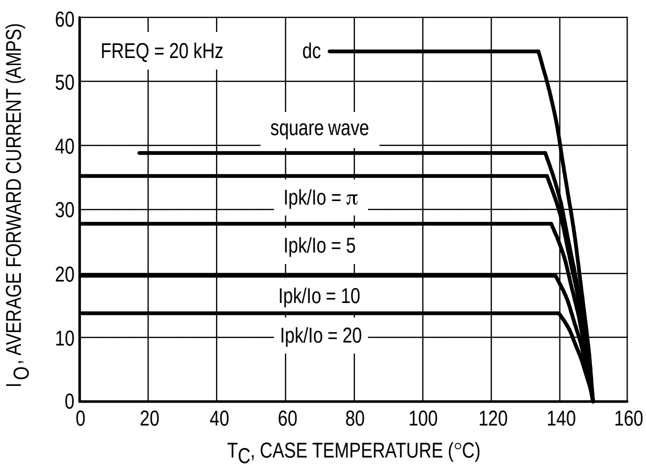


Figure 5. Current Derating (Per Leg)

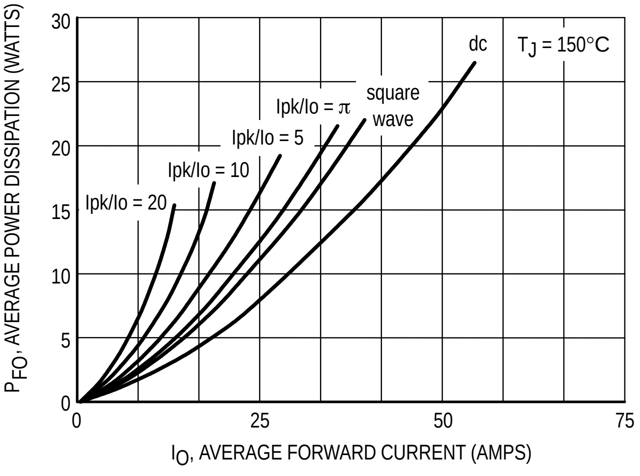


Figure 6. Forward Power Dissipation (Per Leg)

TYPICAL ELECTRICAL CHARACTERISTICS

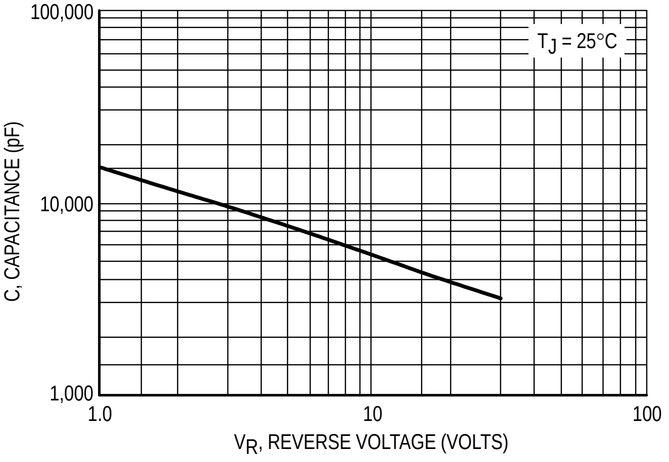


Figure 7. Capacitance

SAFE OPERATING AREA

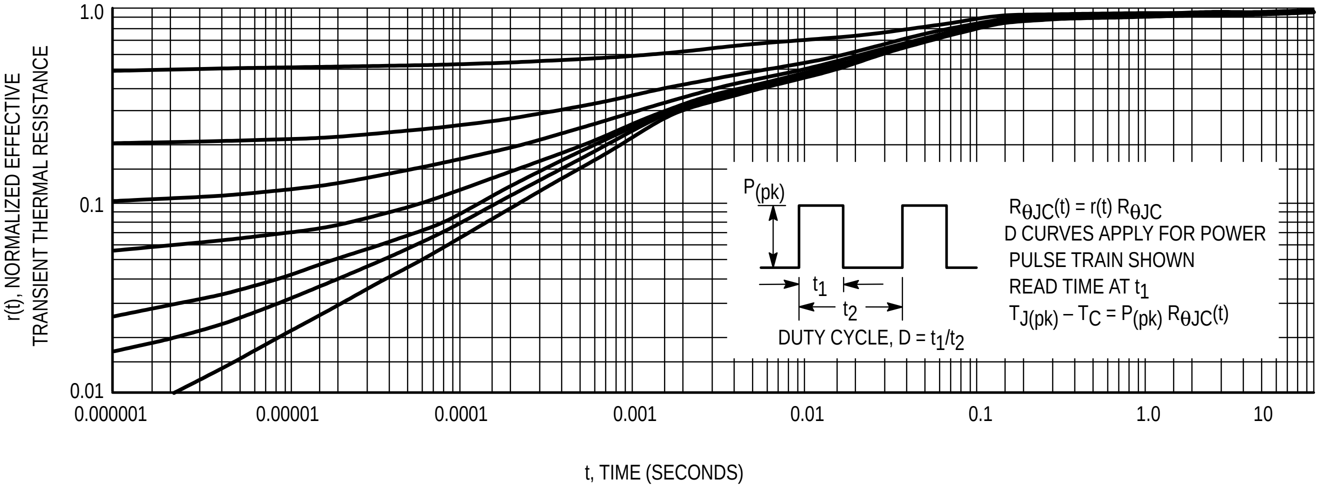


Figure 8. Thermal Response

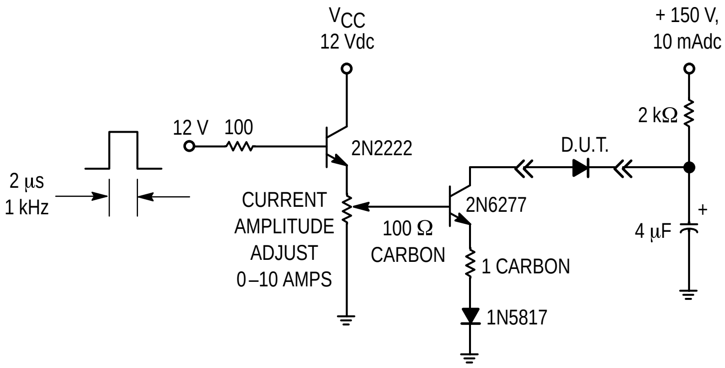
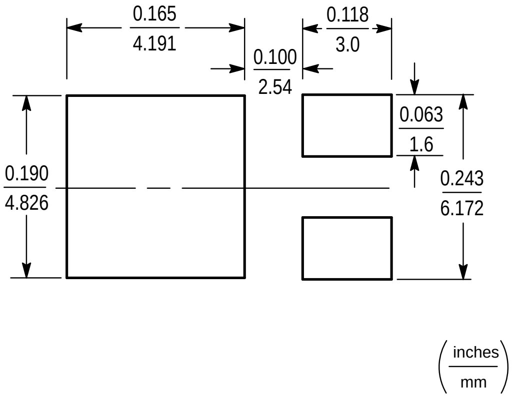


Figure 9. Test Circuit for Repetitive Reverse Current

INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For a D^3PAK device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{54°C/W} = 2.31 \text{ Watts}$$

The 54°C/W for the D^3PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.31 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 11.

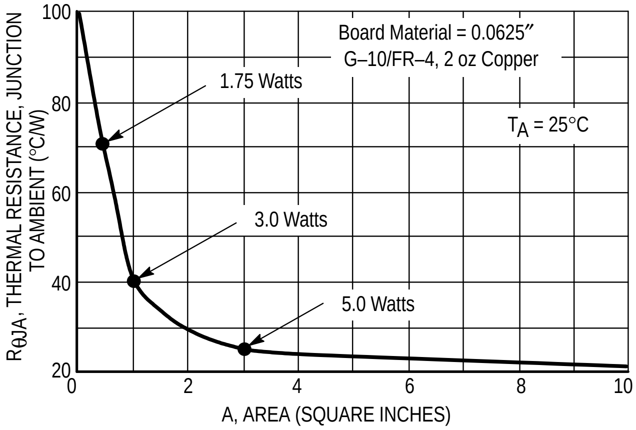


Figure 10. Thermal Resistance versus Drain Pad Area for the D^3PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^{2}PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 12 shows a typical stencil for the DPAK and D^{2}PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

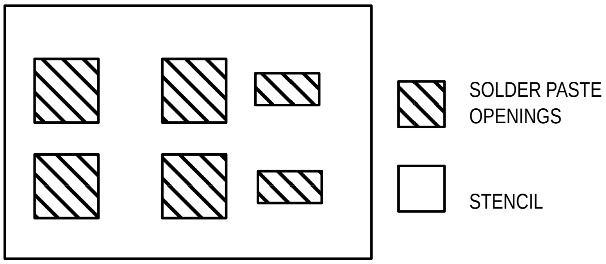


Figure 11. Typical Stencil for DPAK and D^{2}PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^{2}PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

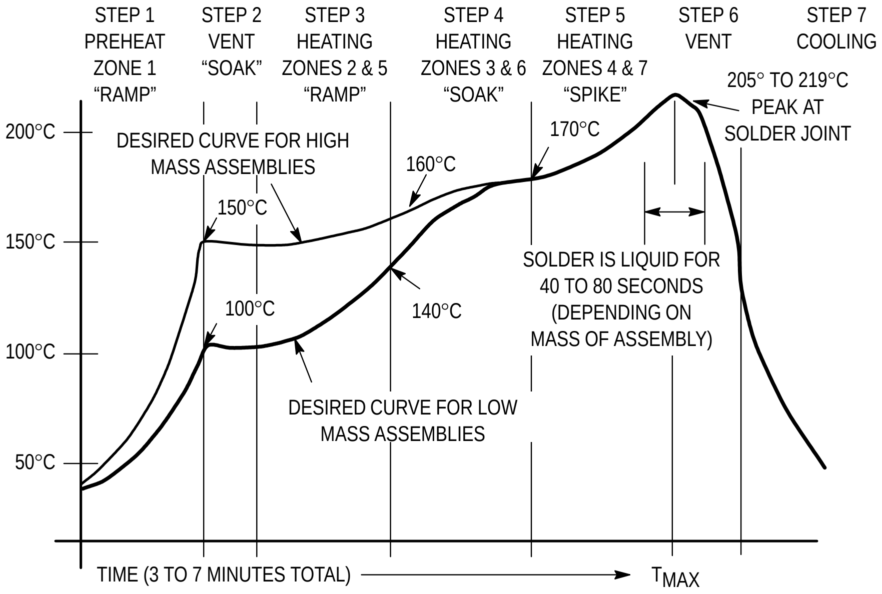
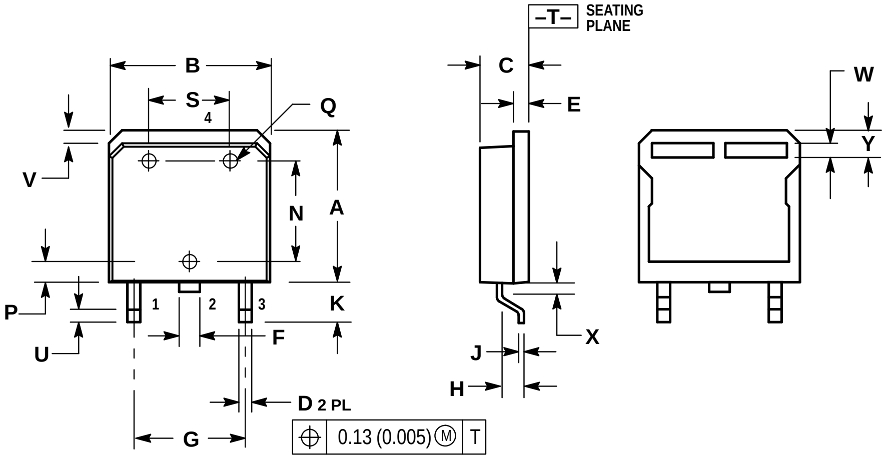


Figure 12. Typical Solder Heating Profile

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.588	0.592	14.94	15.04
B	0.625	0.629	15.88	15.98
C	0.196	0.200	4.98	5.08
D	0.048	0.052	1.22	1.32
E	0.058	0.062	1.47	1.57
F	0.078	0.082	1.98	2.08
G	4.30 BSC		10.92 BSC	
H	0.105	0.110	2.67	2.79
J	0.018	0.022	0.46	0.56
K	0.150	0.160	3.81	4.06
N	0.373	0.377	9.47	9.58
P	0.070	0.074	1.78	1.88
Q	0.054	0.058	1.37	1.47
S	0.313	0.317	7.95	8.05
U	0.050	——	1.27	——
V	0.044	——	1.12	——
W	0.066	0.070	1.68	1.78
X	0.050	0.060	1.27	1.52
Y	0.107	0.111	2.72	2.82

STYLE 1:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

CASE 433A–01
ISSUE A

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