HD74LV175A

Quad. D-type Flip-Flops with Clear

HITACHI

ADE-205-270 (Z)
1st Edition
April 1999

Description

Information at the D inputs of the HD74LV175A is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and common clear. Clearing is accomplished by a negative pulse at the clear input. All four Q outputs are cleared to a logic low level and all four $\overline{Q}$ outputs to a logic high level. Low-voltage and high-speed operation is suitable for battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- V_{CC} = 2.0 V to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.3 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V), ±12 mA (@V_{CC} = 4.5 V to 5.5 V)

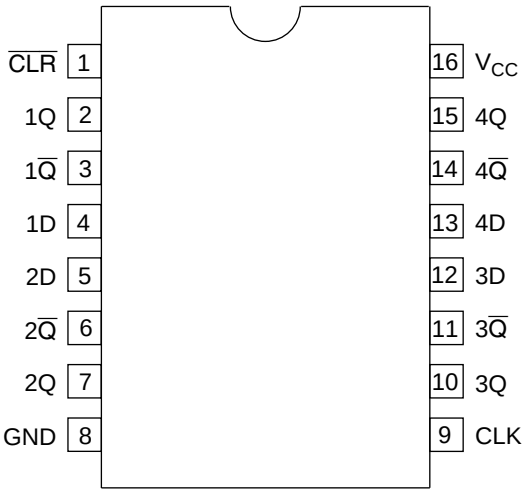
Function Table

Inputs			Outputs	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	↓	X	no change	no change

Note: H: High level
L: Low level
X: Immaterial
↑: Low to high transition
↓: High to low transition

Hitachi semiconductor

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range*[1]	V_I	–0.5 to 7.0	V	
Output voltage range*[1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output: H or L
		–0.5 to 7.0		V_{CC}: OFF
Input clamp current	I_{IK}	–20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air)*[3]	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

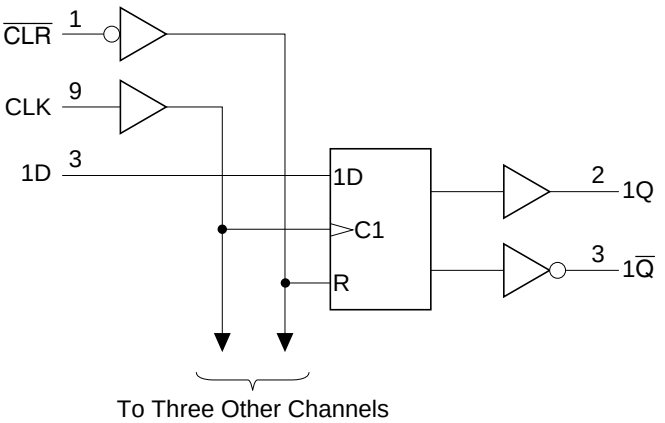
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
Output current	I_{OH}	—	–50	µA	V_{CC} = 2.0 V
		—	–2	mA	V_{CC} = 2.3 to 2.7 V
		—	–6		V_{CC} = 3.0 to 3.6 V
		—	–12		V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	50	µA	V_{CC} = 2.0 V
		—	2	mA	V_{CC} = 2.3 to 2.7 V
		—	6		V_{CC} = 3.0 to 3.6 V
		—	12		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	V_{CC} = 2.3 to 2.7 V
		0	100		V_{CC} = 3.0 to 3.6 V
		0	20		V_{CC} = 4.5 to 5.5 V
Operating free-air temperature	Ta	–40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

- **Ta = –40 to 85°C**

Item	Symbol	V_{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	V_{CC} – 0.1	—	—	V	I_{OH} = –50 µA
		2.3	2.0	—	—		I_{OH} = –2 mA
		3.0	2.48	—	—		I_{OH} = –6 mA
		4.5	3.8	—	—		I_{OH} = –12 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		2.3	—	—	0.4		I_{OL} = 2 mA
		3.0	—	—	0.44		I_{OL} = 6 mA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_I = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	µA	$V_I = V_{CC}$ or GND, I_O = 0
Output leakage current	I_{OFF}	0	—	—	5	µA	V_I or V_O = 0 V to 5.5 V
Input capacitance	C_{IN}	3.3	—	1.4	—	pF	$V_I = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C Min	Typ	Max	Ta = –40 to 85°C Min	Max	Unit	Test Conditions	FROM (Input)	TO (Output)
Maximum clock frequency	fmax	50	105	—	45	—	MHz	C_L = 15 pF		
		40	80	—	35	—		C_L = 50 pF		
Propagation delay time	t_{PLH} / t_{PHL}	—	9.3	18.8	1.0	22.0	ns	C_L = 15 pF	CLK	Q, $\overline{Q}$
		—	12.0	23.3	1.0	27.0		C_L = 50 pF		
	t_{PHL}	—	7.9	16.6	1.0	20.0		C_L = 15 pF	$\overline{CLR}$	
		—	10.4	21.6	1.0	25.5		C_L = 50 pF		
Setup time	t_{SU}	7.0	—	—	7.5	—	ns		Data before CLK↑	
		7.0	—	—	7.5	—			$\overline{CLR}$ inactive before CLK↑	
Hold time	t_h	0.5	—	—	1.0	—	ns		Data after CLK↑	
Pulse width	t_W	6.0	—	—	6.0	—	ns		$\overline{CLR}$ L	
		6.5	—	—	7.0	—			CLK H or L	

Switching Characteristics (cont)

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C Min	Typ	Max	Ta = –40 to 85°C Min	Max	Unit	Test Conditions	FROM (Input)	TO (Output)
Maximum clock frequency	fmax	90	155	—	75	—	MHz	C_L = 15 pF		
		50	120	—	45	—		C_L = 50 pF		
Propagation delay time	t_{PLH} / t_{PHL}	—	6.5	11.5	1.0	13.5	ns	C_L = 15 pF	CLK	Q, $\overline{Q}$
		—	8.4	15.0	1.0	17.0		C_L = 50 pF		
	t_{PLH} / t_{PHL}	—	5.5	10.1	1.0	12.0		C_L = 15 pF	$\overline{CLR}$	
		—	7.4	13.6	1.0	15.5		C_L = 50 pF		
Setup time	t_{SU}	5.0	—	—	5.0	—	ns		Data before CLK↑	
		5.0	—	—	5.0	—			$\overline{CLR}$ inactive before CLK↑	
Hold time	t_h	1.0	—	—	1.0	—	ns		Data after CLK↑	
Pulse width	t_W	5.0	—	—	5.0	—	ns		$\overline{CLR}$ L	
		5.0	—	—	5.0	—			CLK H or L	

Switching Characteristics (cont)

V_{CC} = 5.0 ± 0.5 V

		Ta = 25°C			Ta = –40 to 85°C					
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**FROM (Input)**	**TO (Output)**
Maximum clock frequency	fmax	150	215	—	125	—	MHz	C_L = 15 pF		
		85	165	—	75	—		C_L = 50 pF		
Propagation delay time	t_{PLH} / t_{PHL}	—	4.6	7.3	1.0	8.5	ns	C_L = 15 pF	CLK	Q, $\overline{Q}$
		—	6.0	9.3	1.0	10.5		C_L = 50 pF		
	t_{PLH} / t_{PHL}	—	3.7	6.4	1.0	7.5		C_L = 15 pF	$\overline{CLR}$	
		—	5.3	8.4	1.0	9.5		C_L = 50 pF		
Setup time	t_{SU}	4.0	—	—	4.0	—	ns		Data before CLK↑	
		5.0	—	—	5.0	—			$\overline{CLR}$ inactive before CLK↑	
Hold time	t_h	1.0	—	—	1.0	—	ns		Data after CLK↑	
Pulse width	t_W	5.0	—	—	5.0	—	ns		$\overline{CLR}$ L	
		5.0	—	—	5.0	—			CLK H or L	

Output-skew Characteristics

Item	Symbol	V_{cc} = (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to 85°C Min	Max	Unit
Output skew	$t_{sk\ (O)}$	2.3 to 2.7	—	—	2.0	—	2.0	ns
		3.0 to 3.6	—	—	1.5	—	1.5	
		4.5 to 5.5	—	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

- **C_L = 50 pF**

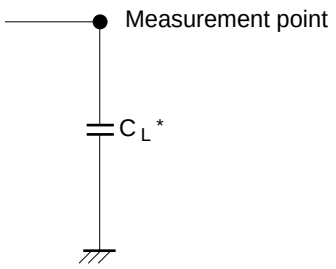
Item	Symbol	V_{cc} = (V)	Ta = 25°C Min	Typ	Max	Unit	Test Conditions
Power dissipation capacitance	C_{PD}	3.3	—	13.6	—	pF	f = 10 MHz
		5.0	—	14.5	—		

Noise Characteristics

- **C_L = 50 pF**

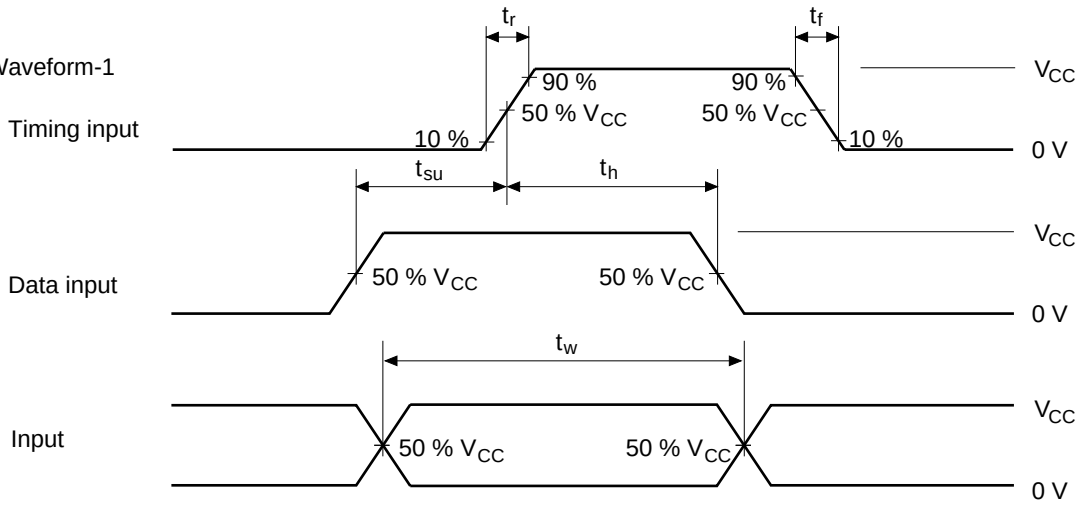
Item	Symbol	V_{cc} = (V)	Ta = 25°C Min	Typ	Max	Unit	Test Conditions
Quiet output, maximum dynamic V_{OL}	$V_{OL\ (P)}$	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL\ (V)}$	3.3	—	–0.3	–0.8		
Quiet output, minimum dynamic V_{OH}	$V_{OH\ (V)}$	3.3	—	3.0	—		
High-level dynamic input voltage	$V_{IH\ (D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL\ (D)}$	3.3	—	—	0.99		

Test Circuit

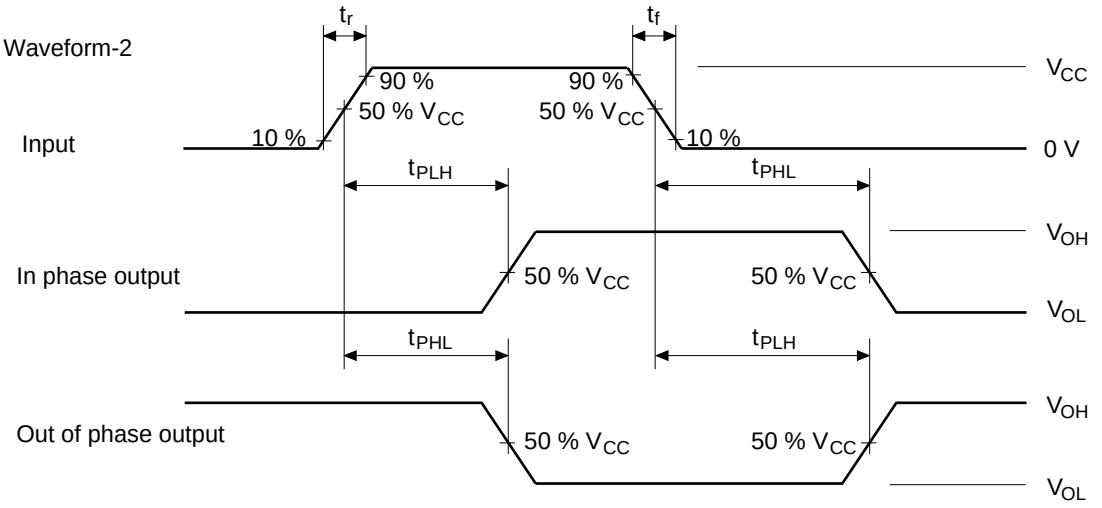


Note: C_L includes the probe and jig capacitance.

• Waveform-1

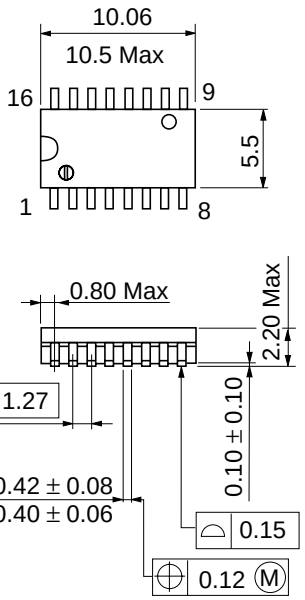


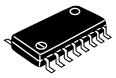
• Waveform-2

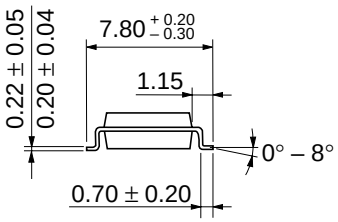


Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, $t_r \leq 3$ ns, $t_f \leq 3$ ns
2. The output is measured one at a time with one transition per measurement.

Package Dimensions



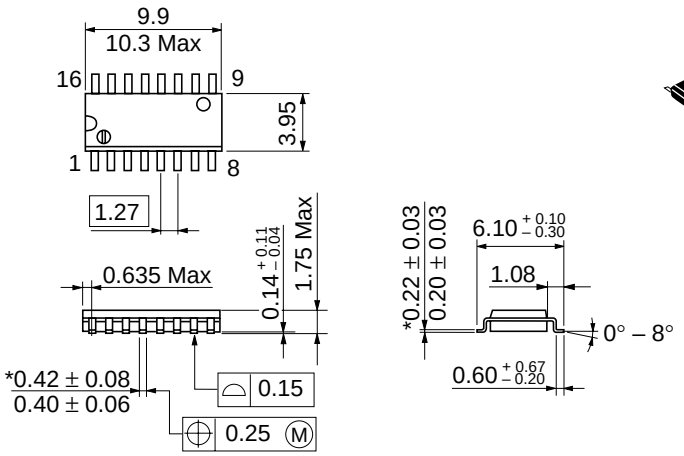




Dimension including the plating thickness
Base material dimension

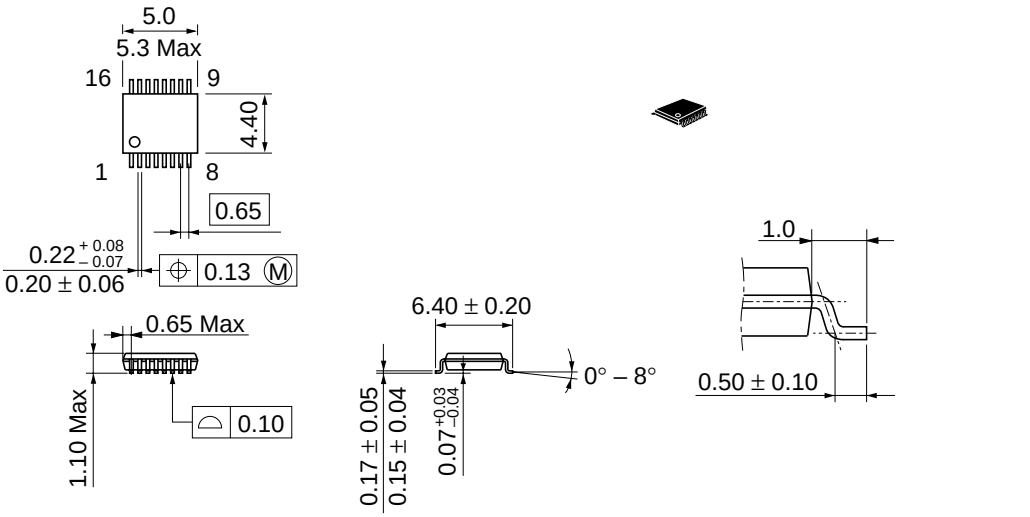
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX