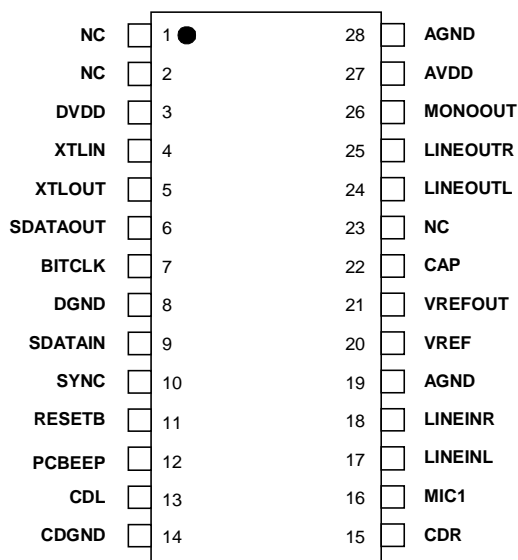




## PIN CONFIGURATION



## ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
XWM9708CDS	0 to 70°C	28-pin SSOP

## PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	NC		No internal connection
2	NC		No internal connection
3	DVDD	Supply	Digital positive supply
4	XTLIN	Digital input	Clock crystal connection or clock input (XTAL not used)
5	XTLOUT	Digital output	Clock crystal connection
6	SDATAOUT	Digital input	Serial data input
7	BITCLK	Digital output	Serial interface clock output to AC'97 controller
8	DGND	Supply	Digital ground supply
9	SDATAIN	Digital output	Serial data output to AC'97 controller
10	SYNC	Digital input	Serial interface sync pulse from AC'97 controller
11	RESETB	Digital input	NOT reset input (active low, resets registers)
12	PCBEEP	Analogue input	Mixer input, typically for PCBEEP signal
13	CDL	Analogue input	Mixer input, typically for CD signal
14	CDGND	Analogue input	CD input common mode reference (ground)
15	CDR	Analogue input	Mixer input, typically for CD signal
16	MIC1	Analogue input	Mixer input with extra gain if required
17	LINEINL	Analogue input	Mixer input, typically for LINE signal
18	LINEINR	Analogue input	Mixer input, typically for LINE signal
19	AGND	Supply	Analogue ground supply, chip substrate
20	VREF	Analogue output	Buffered CAP, used as MIXER reference
21	VREFOUT	Analogue output	Reference for microphones; buffered CAP
22	CAP	Analogue input	Reference input/output; pulls to midrail if not driven
23	NC		No internal connection
24	LINEOUTL	Analogue output	Main analogue output for left channel
25	LINEOUTR	Analogue output	Main analogue output for right channel
26	MONOOUT	Analogue output	Main mono output
27	AVDD	Supply	Analogue positive supply
28	AGND	Supply	Analogue ground supply, chip substrate

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DVSS -0.3V	DVDD +0.3V
Voltage range analogue inputs	AVDD -0.3V	AVDD +0.3V
Operating temperature range, T <sub>A</sub>	0°C	+70°C
Storage prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65 °C	+150°C
Package body temperature (soldering 10 seconds)		+240°C
Package body temperature (soldering 2 minutes)		+183°C

**Note:**

- The digital supply voltage (DVDD) must always be less than or equal to the analogue supply voltage (AVDD).

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		-10%	3.3 to 5.0	+10%	V
Analogue supply range	AVDD		-10%	3.3 to 5.0	+10%	V
Digital ground	DGND			0		V
Analogue ground	AGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Analogue supply current		DVDD, AVDD = 5V		28		mA
Digital supply current		DVDD, AVDD = 5V		22		mA
Standby supply current (all PRs set)		DVDD, AVDD = 5V		10		uA
Analogue supply current		DVDD, AVDD = 3.3V		17		mA
Digital supply current		DVDD, AVDD = 3.3V		13		mA
Standby supply current (all PRs set)		DVDD, AVDD = 3.3V		10		uA

**Note:**

- Both supplies should be powered on and off at the same time.

## ELECTRICAL CHARACTERISTICS

**Test Characteristics:**AVDD = 5V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise statedDVDD = 3.3V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Digital Logic Levels (DVDD = 3.3 or 5.0V)</b>						
Input LOW level	V <sub>IL</sub>		AGND -0.3		0.8	V
Input HIGH level	V <sub>IH</sub>		2.2		AVDD +0.3	V
Output LOW	V <sub>OL</sub>				0.10 x VDD	V
Output HIGH	V <sub>OH</sub>		0.90 x VDD			V
<b>Analogue I/O Levels (Input Signals on any inputs, Outputs on LINEOUT L, R and MONOOUT)</b>						
Input level		Minimum input impedance = 10k	AGND -100mV		AVDD +100mV	V
Output level		Into 10kohm load	AGND +300mV	Near rail to rail	AVDD -300mV	V
<b>Reference Levels</b>						
Reference input/output	CAP2		2/5 AVDD	AVDD/2	3/5 AVDD	V
CAP2 impedance				75		kohms
Mixer reference	VREF			Buffered CAP2		V
MIC reference	VREFOUT			Buffered CAP2		V
MIDBUFF current sink (pins VREF and VREFOUT)		AVDD = 5V	-5	-15		mA
MIDBUFF current source (pins VREF and VREFOUT)		AVDD = 5V	5	15		mA
MIDBUFF current source (pins VREF and VREFOUT)		AVDD = 3.3V		10		mA
MIDBUFF current sink (pins VREF and VREFOUT)		AVDD = 3.3V		-10		mA
<b>DAC Circuit Specifications (AVDD = 5V) 48kHz sampling</b>						
SNR A-weighted (Note 1)			85	95		dBv
Full scale output voltage		VREF = 2.5V		1.0		V <sub>rms</sub>
THD		-3dBfs input	74 (0.02%)	90		dBv
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		40		dB
<b>ADC Circuit Specifications (AVDD = 5V) 48kHz sampling</b>						
SNR A-weighted (Note 1)			75	92		dB
ADC input for full scale output		VREF = 2.5V		1.0		V <sub>rms</sub>
THD		-6dBv input	74	95		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74			dB
PSRR		20 to 20kHz		40		dB

**Test Characteristics:**AVDD = 5V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise statedDVDD = 3.3V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Mixer Circuit Specifications (AVDD = 5V) 48kHz sampling</b>						
SNR CD path A-weighted (Note 1)			90	100		dB
SNR Other paths A-weighted (Note 1)			85	95		dB
Maximum input voltage			AGND	1.0	AVDD	V <sub>rms</sub>
Maximum output voltage on LINEOUT			1.0	1.8		V <sub>rms</sub>
THD		0dBv input	74	90		dB
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain		15		kohm
Input impedance (other mixer inputs)		At max gain	10	20		kohm
		At 0db gain	50	100		kohm
Input impedance MIC inputs		At max gain	10	30		kohm
		At 0db gain	55	110		kohm
PSRR		20 to 20kHz		50		dB
<b>DAC Circuit Specifications (AVDD = 3.3V) 48kHz sampling</b>						
SNR A-weighted (Note 1)				92		dB
Full scale output voltage		VREF = 1.65V		0.7		V <sub>rms</sub>
THD		-3dBFS input		85		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		40		dB
<b>ADC Circuit Specifications (AVDD = 3.3V) 48kHz sampling</b>						
SNR A-weighted (Note 1)				85		dB
ADC input for full scale output		VREF = 1.65V		0.7		V <sub>rms</sub>
THD		-6dBv input		80		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74			dB
PSRR		20 to 20kHz		40		dB

**Test Characteristics:**

AVDD = 5V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated

DVDD = 3.3V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Mixer Circuit Specifications (AVDD = 3.3V) 48kHz sampling</b>						
SNR CD path A-weighted (Note 1)				95		dB
SNR Other paths A-weighted (Note 1)				90		dB
Maximum input voltage				0.6		V <sub>rms</sub>
Maximum output voltage on LINEOUT				1.2		V <sub>rms</sub>
THD (Note 2)		-3.6dBv input		85		dBv
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain		15		kohm
Input impedance (other Mixer inputs)		At max gain		20		kohm
		At 0db gain		100		kohm
Input impedance MIC inputs		At max gain		30		kohm
		At 0db gain		110		kohm
PSRR		20 to 20kHz		50		dB
<b>Clock Frequency Range</b>						
Crystal clock				24.576		MHz
BITCLK frequency				12.288		MHz
SYNC frequency				48.0		kHz

**Notes:**

1. SNR is the ratio of 0dB signal output to the output level with no signal, measured A-weighted over a 20Hz to 20kHz bandwidth.
2. Inputs are scaled for AVDD eg; 0dBv at 5.0V is equivalent to -3.6dBv at 3.3V.

## DETAILED TIMING DIAGRAMS

### Test Characteristics:

AVDD = 5V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated.  
 DVDD = 3.3V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated.  
 All measurements are taken at 10% to 90% VDD, unless otherwise stated. All the following timing information is guaranteed, not tested.

### AC-LINK LOW POWER MODE

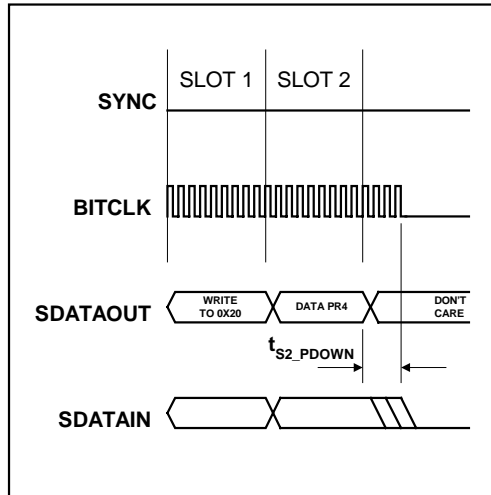


Figure 1 AC-Link Powerdown Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
End of slot 2 to BITCLK SDATIN low	$t_{S2\_PDOWN}$			1.0	$\mu$ s

### COLD RESET

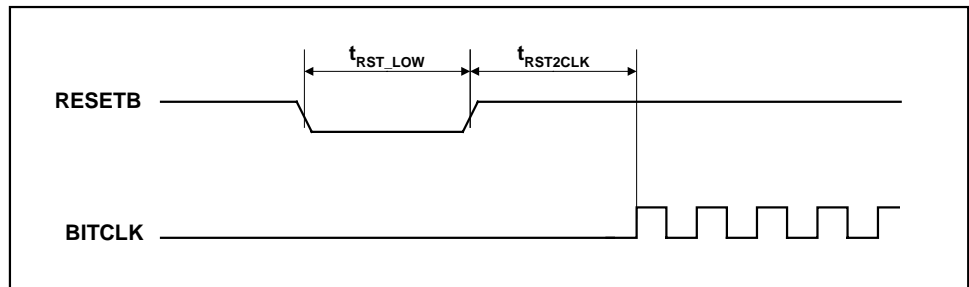
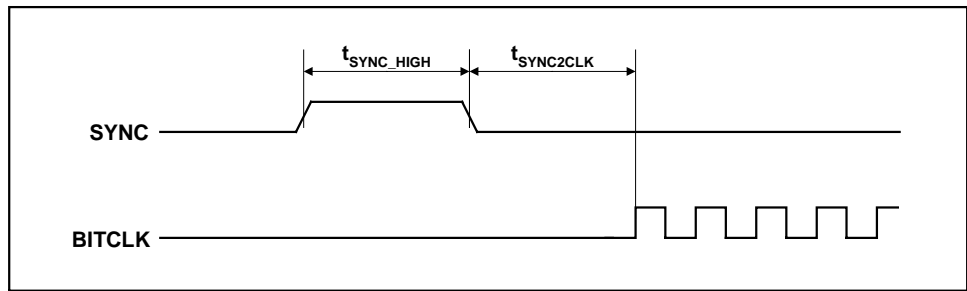


Figure 2 Cold Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESETB active low pulse width	$t_{RST\_LOW}$	1.0			$\mu$ s
RESETB release (or rising edge) to BITCLK startup delay	$t_{RST2\_CLK}$	162.8			ns

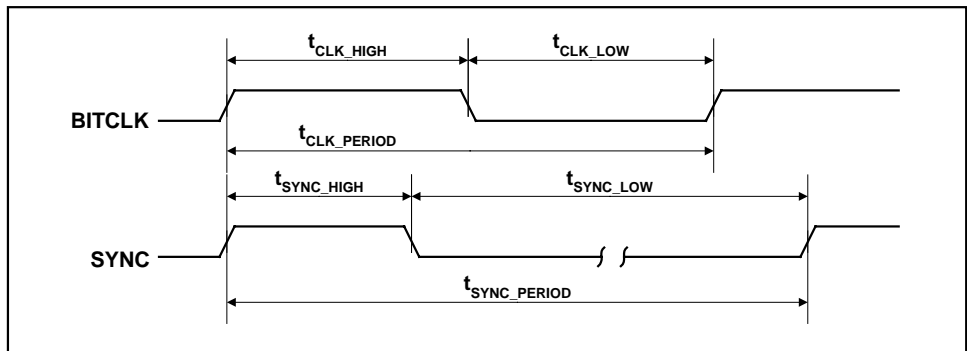
**WARM RESET**



**Figure 3 Warm Reset Timing**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SYNC active high pulse width	$t_{\text{SYNC\_HIGH}}$		1.3		$\mu\text{s}$
SYNC release (or falling edge) to BITCLK startup delay	$t_{\text{SYNC2\_CLK}}$	162.4			ns

**CLOCK SPECIFICATIONS**



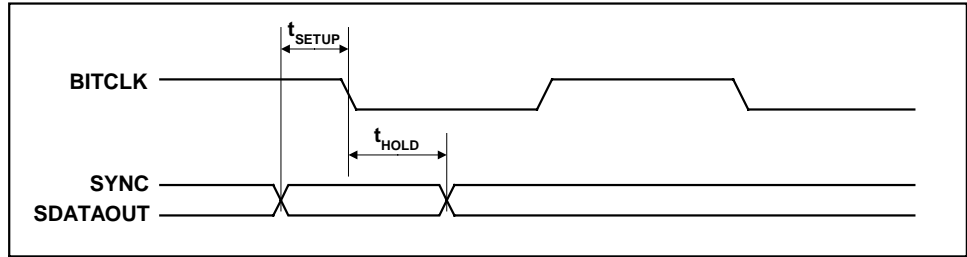
**Figure 4 Clock Specifications (50pF External Load)**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK frequency			12.288		MHz
BITCLK period	$t_{\text{CLK\_PERIOD}}$		81.4		ns
BITCLK output jitter				750	ps
BITCLK high pulse width (See Note)	$t_{\text{CLK\_HIGH}}$	32.56	40.7	48.84	ns
BITCLK low pulse width (See Note)	$t_{\text{CLK\_LOW}}$	32.56	40.7	48.84	ns
SYNC frequency			48.0		kHz
SYNC period	$t_{\text{SYNC\_PERIOD}}$		20.8		$\mu\text{s}$
SYNC high pulse width	$t_{\text{SYNC\_HIGH}}$		1.3		$\mu\text{s}$
SYNC low pulse width	$t_{\text{SYNC\_LOW}}$		19.5		$\mu\text{s}$

**Note:** Worst case duty cycle restricted to 40/60.



**DATA SETUP AND HOLD (50pF EXTERNAL LOAD)**

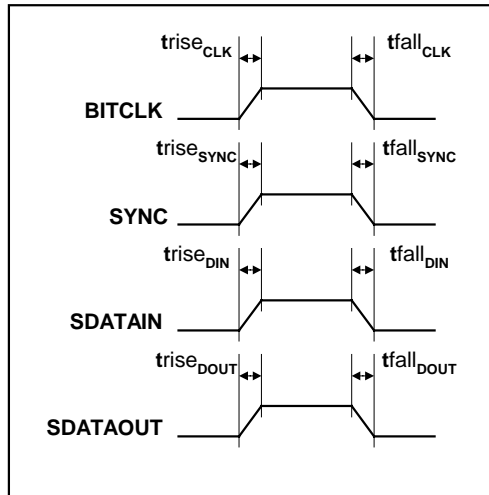


**Figure 5 Data Setup and Hold (50pF External Load)**

**Note:** Setup and hold time parameters for SDATA\_IN are with respect to AC'97 Controller.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to falling edge of BITCLK	$t_{SETUP}$	15.0			ns
Hold from falling edge of BITCLK	$t_{HOLD}$	5.0			ns

**SIGNAL RISE AND FALL TIMES**



**Figure 6 Signal Rise and Fall Times (50pF external load)**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK rise time	$trise_{CLK}$	2		6	ns
BITCLK fall time	$tfall_{CLK}$	2		6	ns
SYNC rise time	$trise_{SYNC}$	2		6	ns
SYNC fall time	$tfall_{SYNC}$	2		6	ns
SDATAIN rise time	$trise_{DIN}$	2		6	ns
SDATAIN fall time	$trise_{DIN}$	2		6	ns
SDATAOUT rise time	$trise_{DOUT}$	2		6	ns
SDATAOUT fall time	$tfall_{DOUT}$	2		6	ns

## SYSTEM INFORMATION

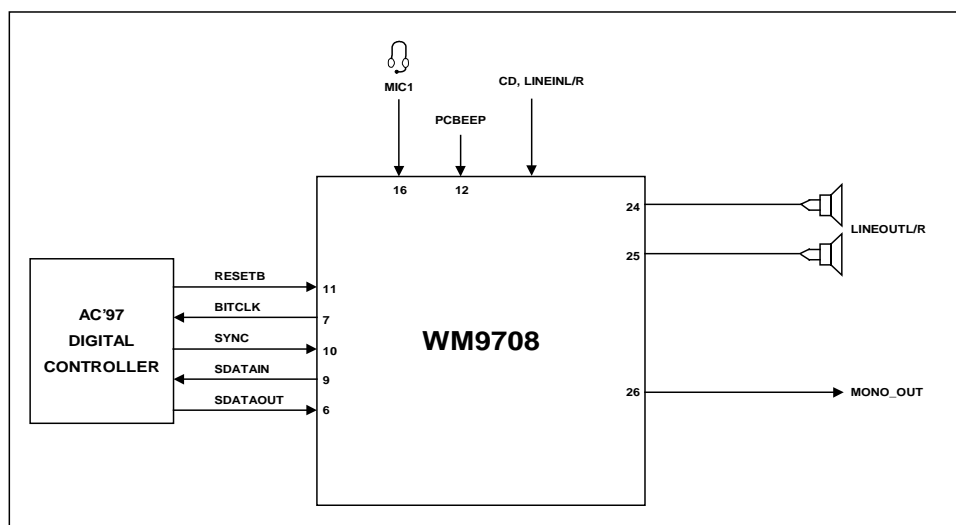


Figure 7 Revision 2.1 Compliant 2-Channel Codec

## DEVICE DESCRIPTION

### INTRODUCTION

The WM9708 comprises a stereo 18-bit Codec, (that is, 2 ADCs and 2 DACs) a comprehensive analogue mixer with 2 sets of stereo inputs, phone, microphone, and PC-beep inputs. Additionally, on-chip reference generation circuits generate the necessary bias voltages for the device, and a bi-directional serial interface allows transfer of control data and DAC and ADC words to and from the AC'97 controller. The WM9708 supports 18-bit resolution within the DAC and ADC functions, but the AC'97 serial interface specification allows any word length up to 20-bits to be written to, or read from, the AC'97 Codec. These words are MSB justified, and any LSBs not used will simply default to 0. Normally it is anticipated that 16-bit words will be used in most PC type systems. Therefore, for the DAC, 16-bit words will be downloaded into the Codec from the controller, along with padding of 0s to make the 16-bit word up to 20-bit length. In this case, the WM9708 will process the 16-bit word along with 0 padding bits in the 2 LSB locations (to make 18-bit). At the ADC output, WM9708 will provide an 18-bit word, again with 0s in the two LSB locations (20-bit). The AC'97 controller will then ignore the 4 LSBs of the 20-bit word. When the WM9708 is interrogated at Register 00h, it responds indicating it is an 18-bit device.

The WM9708 has the ADC and DAC functions implemented using oversampled, or sigma-delta converters, and uses on-chip digital filters to convert these 1-bit signals to and from the 48ks/s 16/18-bit PCM words that the AC'97 controller requires. The digital parts of the device are powered separately from the analogue to optimise performance, and 3.3V digital and 5V analogue supplies may be used on the same device to further optimise performance. Digital I/Os are 5V tolerant when the analogue supplies are 5V, so the WM9708 may be connected to a controller running on 5V supplies, but use 3.3V for the digital section of WM9708. WM9708 is also capable of operating with a 3.3V supply only (digital and analogue).

An internally generated midrail reference is provided at pin CAP which is used as the chip reference. This pin should be heavily decoupled. Refer to Figure 15 for more details.

The WM9708 is not limited to PC-only applications. The ability to power down sections of the device selectively, and the option to choose alternative master clock, and hence sample rates, means that many alternative applications in areas such as telecoms, may be anticipated.

Additional features added to the Intel AC'97 2.1 specification, such as the internal connection of PC-beep to the outputs in the case where the device is reset, are supported, along with optional features such as variable sample rate support.

## VARIABLE SAMPLE RATE SUPPORT

The DACs and ADCs on this device support all the recommended sample rates specified in the Intel Revision 2.1 specification for audio rates. The default rate is 48ks/s. If alternative rates are selected and variable rate audio is enabled (Register 2Ah, bit 0), the AC'97 interface continues to run at 48k words per second, but data is transferred across the link in bursts such that the net sample rate selected is achieved. It is up to the AC'97 Revision 2.1 compliant controller to ensure that data is supplied to the AC link, and received from the AC link, at the appropriate rate.

The device supports on demand sampling. That is, when the DAC signal processing circuits need another sample, a sample request is sent to the controller which must respond with a data sample in the next frame it sends. For example, if a rate of 24ks/s is selected, on average the device will request a sample from the controller every other frame, for each of the stereo DACs. Note that if an unsupported rate is written to one of the rate registers, the rate will default to the nearest rate supported. The Register will then respond when interrogated with the default sample rate.

The left and right channels of the ADCs and DACs always sample at the same rate.

AUDIO SAMPLE RATE	CONTROL VALUE D15-D0
8000	1F40
11025	2B11
16000	3E80
22050	5622
32000	7D00
44100	AC44
48000	BB80

**Table 1 Variable Sample Rates Supported**

## GAIN CONTROL REGISTER LOCATION

PGA	CONTROL REGISTER	MUTE DEFAULT
DAC	18h	Muted (bit-15)
Mixer	72h	Not-muted (bit-15)
Volume	02h	Muted (15)

**Table 2 Gain Control Register Location**

## MASTER SUPPORT

WM9708 supports operation as a master codec. Fundamentally, a device identified as a master produces a BITCLK as an input.

## CONTROL INTERFACE

A digital interface has been provided to control the WM9708 and transfer data to and from it. This serial interface is compatible with the Intel AC'97 specification.

The main control interface functions are:

- Control of analogue gain and signal paths through the mixer
- Bi-directional transfer of ADC and DAC words to and from AC'97 controller
- Selection of Powerdown down modes.

**AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL**

The WM9708 incorporates a 5-pin digital serial interface that links it to the AC'97 controller. The AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control Register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution and a 16-bit header slot. With a minimum required DAC and ADC resolution of 16-bits, AC'97 may also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides. The WM9708 provides support for 18-bit operation.

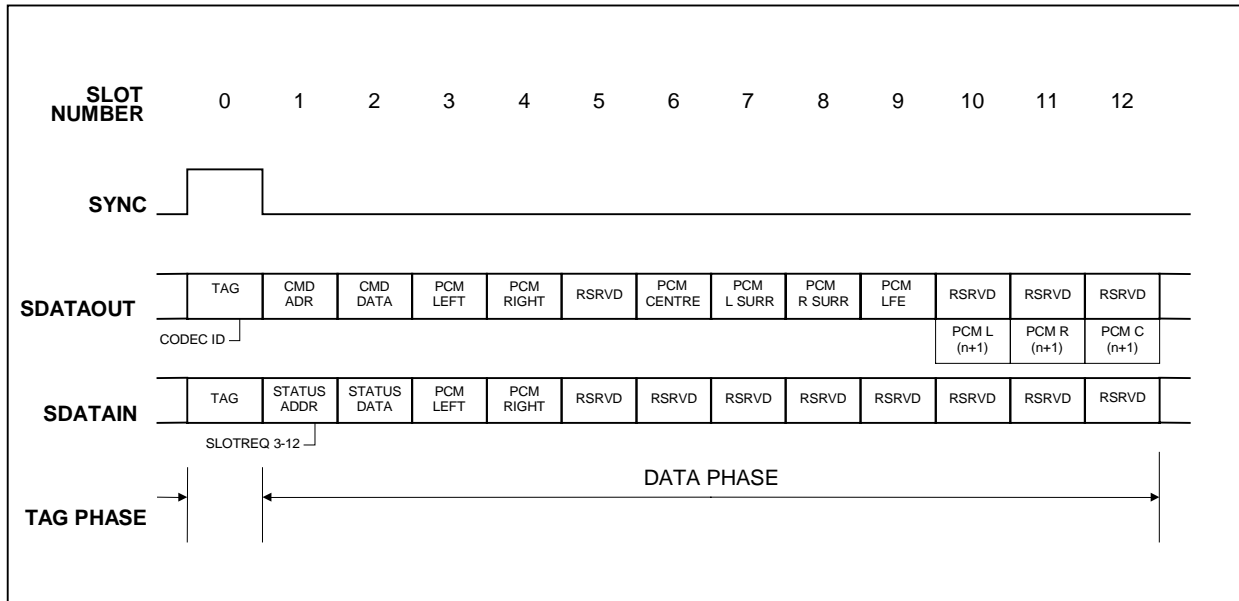


Figure 8 AC'97 Standard Bi-directional Audio Frame

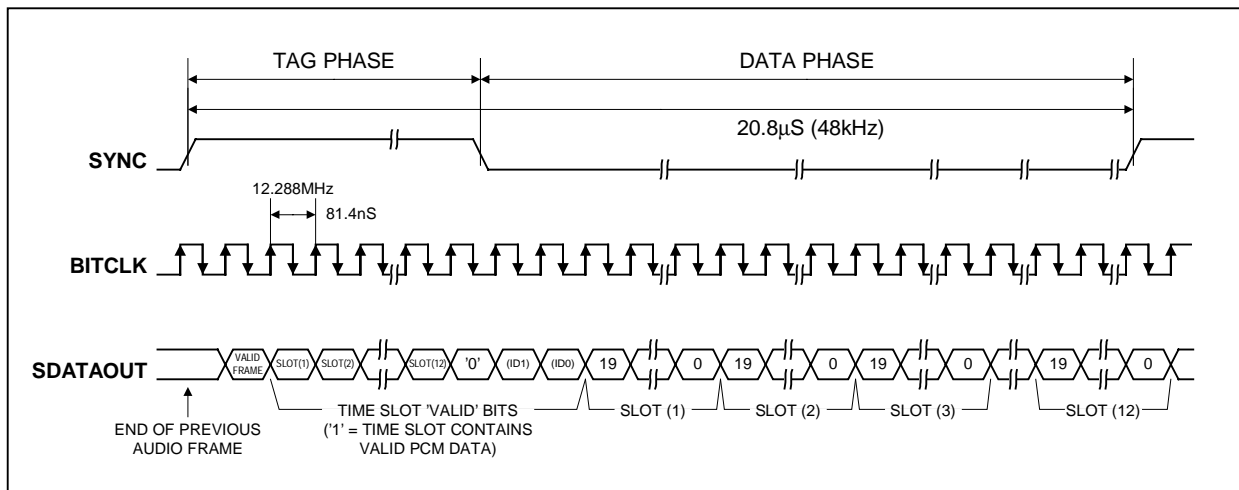


Figure 9 AC-link Audio Output Frame

The datastreams currently defined by the AC'97 specification include:

<b>PCM playback - 2 output slots</b>	2-channel composite PCM output stream
<b>PCM record data - 2 input slots</b>	2-channel composite PCM input stream
<b>Control - 2 output slots</b>	Control Register write port
<b>Status - 2 input slots</b>	Control Register read port
<b>Optional modem line codec output - 1 output slot</b>	Modem line codec DAC input stream
<b>Optional modem line codec input - 1 input slot</b>	Modem line codec ADC output stream
<b>Optional dedicated microphone input - 1 input slot</b>	Dedicated microphone input stream in support of stereo AEC and/or other voice applications.

Synchronisation of all AC-link data transactions is signalled by the WM9708 controller. The WM9708 drives the serial bit clock onto AC-link, which the AC'97 controller then qualifies with a synchronisation signal to construct audio frames.

SYNC, fixed at 48kHz, is derived by dividing down the serial clock (BITCLK). BITCLK, fixed at 12.288MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots and the tag slot. AC-link serial data is transitioned on each rising edge of BITCLK. The receiver of AC-link data, (WM9708 for outgoing data and AC'97 controller for incoming data), samples each serial bit on the falling edges of BITCLK.

The AC-link protocol provides for a special 16-bit time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (the WM9708 for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BITCLKs at the beginning of each audio frame.

The portion of the audio frame where SYNC is high is defined as the Tag Phase. The remainder of the audio frame where SYNC is low is defined as the Data Phase. Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that the WM9708 be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

## AC-LINK AUDIO OUTPUT FRAME (SDATA\_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the WM9708's DAC inputs, and control registers. As briefly mentioned earlier, each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

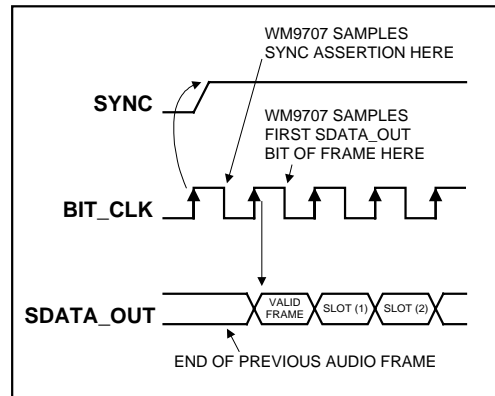
### OUTPUT TAG SLOT (16-BITS)

Bit (15)	Frame Valid
Bit (14)	Slot 1 Valid Command Address bit (Primary Codec only)
Bit (13)	Slot 2 Valid Command Data bit (Primary Codec only)
Bit (12:3)	Slot 3-12 Valid bits as defined by AC'97
Bit 2	Reserved (Set to 0)
Bit (1:0)	2-bit Message ID field (00 reserved for Primary; 01 indicates Secondary)

Within slot 0 the first bit is a global bit (SDATAOUT slot 0, bit 15) which flags the validity for the entire audio frame. If the Valid Frame bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12-bit positions sampled by the WM9708 indicate which of the corresponding 12 time slots contain valid data. It should be noted that in URA, even when slot 1 is tagged as invalid, the request bits are still valid.

In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48kHz audio frame rate. Figure 9 illustrates the time slot based AC-link protocol.

When the Codec is a slave device, bits 14 and 13 are not used to validate data in slots 1 and 2. Instead, if the message ID bits (1:0) match the Codec ID then the address is valid and bit 19 from slot 1 then indicates if slot 2 is valid.



**Figure 10 Start of an Audio Output Frame**

A new audio output frame begins with a low to high transition of SYNC as shown in Figure 10. SYNC is synchronous to the rising edge of BITCLK. On the immediately following falling edge of BITCLK, the WM9708 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BITCLK, AC'97 transitions SDATAOUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BITCLK, and subsequently sampled by the WM9708 on the following falling edge of BITCLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Baseline AC'97 specified audio functionality MUST ALWAYS sample rate convert to and from a fixed 48ks/s on the AC'97 controller. This requirement is necessary to ensure that interoperability between the AC'97 controller and the WM9708, among other things, can be guaranteed by definition for baseline specified AC'97 features.

SDATAOUT's composite stream is MSB justified (MSB first) with all non-valid slot bit positions stuffed with 0s by the AC'97 controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the AC'97 controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0s.

As an example, consider an 8-bit sample stream that is being played out to one of the WM9708's DACs. The first 8 bit positions are presented to the DAC (MSB justified) followed by the next 12 bit positions, which are stuffed with 0s by the AC'97 controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC'97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

### SLOT 1: COMMAND ADDRESS PORT

The command port is used to control features, and monitor status for the WM9708 functions including, but not limited to, mixer settings, and power management (refer to the Serial Interface Register Map). The control interface architecture supports up to 128, 16-bit read/write registers, however only those addressable on even byte boundaries are used in Rev 2.1. Only the even Registers (00h, 02h, etc.) are valid. Odd register read/write will have no effect on the WM9708.

Audio output frame slot 1 communicates control register address, and read/write command information to the WM9708.

#### COMMAND ADDRESS PORT BIT ASSIGNMENTS

Bit (19)	Read/write command (1 = read, 0 = write)
Bit (18:12)	Control register index (64 16-bit locations, addressed on even byte boundaries)
Bit (11:0)	Reserved (stuffed with 0s)

The first bit (MSB) sampled by the WM9708 indicates whether the current control transaction is a read or write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0s by the AC'97 controller.

### SLOT 2: COMMAND DATA PORT

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (As indicated by slot 1, bit 19).

Bit (19:4)	Control register write data (stuffed with 0s if current operation is a read)
Bit (3:0)	Reserved (stuffed with 0s)

If the current command port operation is a read then the entire time slot must be stuffed with 0s by the AC'97 controller.

### SLOT 3: PCM PLAYBACK LEFT CHANNEL

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical Games Compatible PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

### SLOT 4: PCM PLAYBACK RIGHT CHANNEL

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical Games Compatible PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples.

If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

### SLOT 5: OPTIONAL MODEM LINE CODEC

Audio output frame slot 5 contains the MSB justified modem DAC input data. This optional AC'97 feature is not supported in the WM9708, and if data is written to this location it is ignored. This may be determined by the AC'97 controller interrogating the WM9708 reg 28h and 3Ch.

**SLOTS 6 TO 9: SURROUND SOUND DATA**

Audio output frame slots 6 to 9 are used to send surround sound data. Unsupported by WM9708.

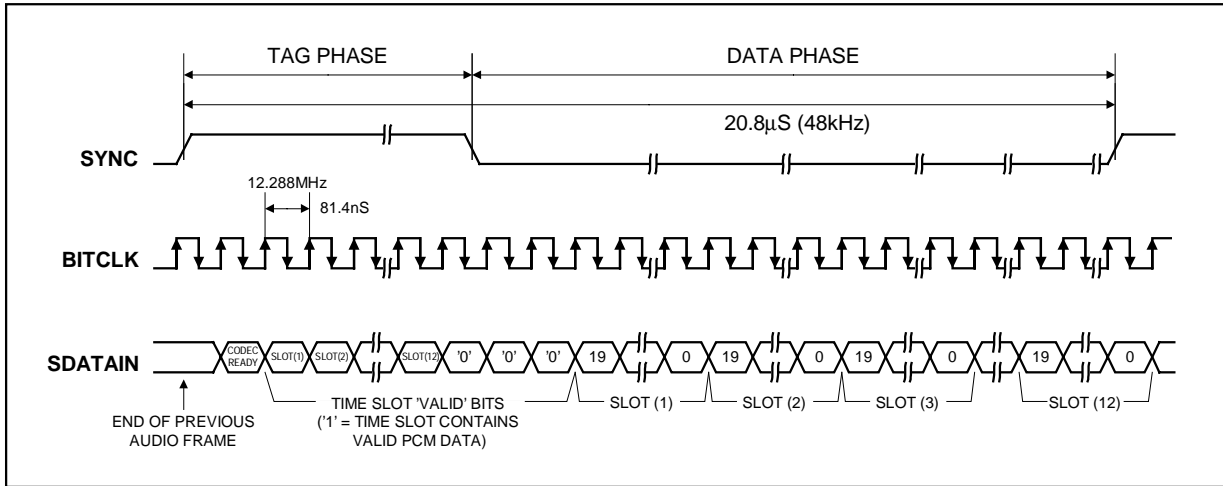
**SLOTS 10 AND 11: LINE2 AND HANDSET DAC**

These data slots are not supported.

**SLOT 12: GPIO CONTROL**

These data slots are not supported.

**AC-LINK AUDIO INPUT FRAME (SDATA\_IN)**



**Figure 11 AC-link Audio Input Frame**

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots plus the tag slot.

Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

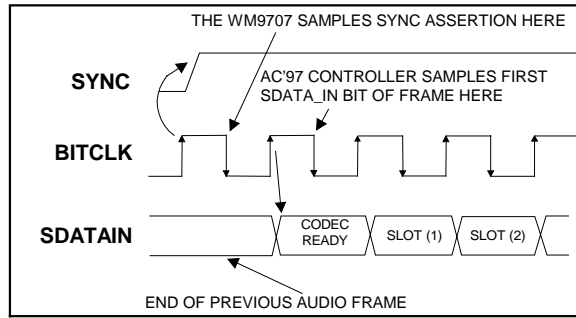
Within slot 0 the first bit is a global bit (SDATAIN slot 0, bit 15) which flags whether the WM9708 is in the Codec Ready state or not. If the Codec Ready bit is a 0, this indicates that the WM9708 is not ready for normal operation. This condition is normal following the desertion of power on reset for example, while the WM9708's voltage references settle. When the AC-link Codec Ready indicator bit is a 1, it indicates that the AC-link and the WM9708 control and status registers are in a fully operational state. The AC'97 controller must further probe the Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting the WM9708 into operation the AC'97 controller should poll the first bit in the audio input frame (SDATAIN slot 0, bit 15) for an indication that the WM9708 has gone Codec Ready.

Once the WM9708 is sampled Codec Ready then the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 11 illustrates the time slot based AC-link protocol.

There are several subsections within the WM9708 that can independently go busy/ready. It is the responsibility of the WM9708 controller to probe more deeply into the WM9708 register file to determine which the WM9708 subsections are actually ready.





**Figure 12 Start of an Audio Input Frame**

A new audio input frame begins with a low to high transition of SYNC as shown in Figure 12. SYNC is incident with the rising edge of BITCLK. On the immediately following falling edge of BITCLK, AC'97 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BITCLK, AC'97 transitions SDATAIN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BITCLK, and subsequently sampled by the AC'97 Controller on the following falling edge of BITCLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDATAIN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0s by the WM9708. SDATAIN should be sampled on the falling edges of BITCLK.

**SLOT 1: STATUS ADDRESS PORT**

The status port is used to monitor status for the WM9708 functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1 echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged valid by the WM9708 during slot 0).

**STATUS ADDRESS PORT BIT ASSIGNMENTS:**

Bit (19)	RESERVED (stuffed with 0s)
Bit (18:12)	Control register index (echo of register index for which data is being returned)
Bit (11:2)	Variable sample rate SLOTREQ bits.
Bit (1:0)	RESERVED (stuffed with 0s)

The first bit (MSB) generated by the WM9708 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address. The next 10 bits support the AC'97 Rev 2.1 variable sample rate signalling protocol, and the trailing 2 bit positions are stuffed with 0s by AC'97.

In VRA the slot requests in slot 1 (bits 11-3) are always valid regardless of slot tag.

**SLOT 2: STATUS DATA PORT**

The status data port delivers 16-bit control register read data.

Bit (19:4)	Control register read data (stuffed with 0s if tagged invalid by WM9701)
Bit (3:0)	RESERVED (stuffed with 0s)

If slot 2 is tagged invalid by the WM9708, then the entire slot will be stuffed with 0s by the WM9708.

**SLOT 3: PCM RECORD LEFT CHANNEL**

Audio input frame slot 3 is the left channel output of the WM9708's input Mux, post-ADC.

The WM9708 sends out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

**SLOT 4: PCM RECORD RIGHT CHANNEL**

Audio input frame slot 4 is the right channel output of the WM9708's input Mux, post-ADC.

The WM9708's ADCs can be implemented to support 16, 18, or 20-bit resolution.

The WM9708 ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

**SLOT 5: OPTIONAL MODEM LINE CODEC**

Not supported by WM9708.

**SLOT 6: OPTIONAL DEDICATED MICROPHONE RECORD DATA**

Not supported by WM9708.

**SLOTS 7 TO 12: RESERVED**

Audio input frame slots 7 to 12 are reserved for future use and are always stuffed with 0s by the WM9708.

**AC-LINK LOW POWER MODE**

The AC-link signals can be placed in a low power mode. When the WM9708's Powerdown Register 26h, is programmed to the appropriate value, both BITCLK and SDATAIN will be brought to, and held at a logic low voltage level.

BITCLK and SDATAIN are transitioned low immediately following the decode of the write to the Powerdown Register 26h with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame. At this point in time it is strongly recommended that all sources of audio input have also been neutralised.

The AC'97 controller should also drive SYNC and SDATAOUT low after programming the WM9708 to this low power, halted mode.

Once the WM9708 has been instructed to halt BITCLK, a special wake up protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BITCLK.

**WAKING UP THE AC-LINK**

There are 2 methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC'97 controller that performs the wake up task.

AC-link protocol provides for a Cold WM9708 Reset, and a Warm WM9708 Reset.

The current Powerdown state would ultimately dictate which form of WM9708 reset is appropriate. Unless a cold or register reset (a write to the Reset Register 00h) is performed, wherein the WM9708 registers are initialised to their default values, registers are required to keep state during all Powerdown modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the Powerdown was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

**COLD WM9708 RESET**

A cold reset is achieved by asserting RESETB for the minimum specified time (1 $\mu$ s). By driving RESETB low, BITCLK, and SDATAOUT will be activated, or re-activated as the case may be, and all the WM9708 control registers will be initialised to their default power on reset values.

RESETB is an asynchronous WM9708 input. See Figure 2.

### WARM WM9708 RESET

A warm WM9708 reset will re-activate the AC-link without altering the current WM9708 register values. A warm reset is signalled by driving SYNC high for a minimum of 1µs in the absence of BITCLK. See Figure 3.

Within normal audio frames SYNC is a synchronous input. In the absence of BITCLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the WM9708. The WM9708 will not respond with the activation of BITCLK until SYNC has been sampled low again by the WM9708. This will preclude the false detection of a new audio frame.

## SERIAL INTERFACE REGISTER MAP DESCRIPTION

(See Table 15)

The serial interface bits perform control functions described as follows: The register map is fully specified by the AC'97 specification, and this description is simply repeated below, with optional unsupported features omitted.

### RESET REGISTER (INDEX 00h)

Writing any value to this register performs a register reset, which causes registers 0-2B inclusive to revert to their default values. Reading this register returns the ID code of the part, indication of modem support (not supported by the WM9708) and a code for the type of 3D stereo enhancement (not supported by the WM9708).

The ID decodes the capabilities of the WM9708 based on the following:

BIT	FUNCTION	VALUE ON WM9708
ID0	Dedicated Mic PCM in channel	0
ID1	Modem line codec support	0
ID2	Bass and treble control	0
ID3	Simulated stereo (mono to stereo)	0
ID4	Headphone out support	1
ID5	Loudness (bass boost) support	0
ID6	18-bit DAC resolution	1
ID7	20-bit DAC resolution	0
ID8	18-bit ADC resolution	1
ID9	20-bit ADC resolution	0
SE4...SE0	No 3D support	00000

**Table 3 Reset Register Function**

Note that the WM9708 defaults to indicate 18-bit compatibility.

### PLAY MASTER VOLUME REGISTERS (INDEX 02h, 04h AND 06h)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), Register 04h controls the optional stereo headphone out, and Register 06h controls the mono volume output. Each step corresponds to 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at  $-\infty$ dB.

ML5 to ML0 is for left channel level, MR5 to MR0 is for the right channel and MM5 to MM0 is for the mono out channel.

Support for the MSB of the volume level is not provided by the WM9708. If the MSB is written to, then the WM9708 detects when that bit is set and sets all 4 LSBs to 1s. Example: If the driver writes a 1xxxx the WM9708 interprets that as x11111. It will also respond when read with x11111 rather than 1xxxx, the value written to it. The driver can use this feature to detect if support for the 6th bit is there or not.

The default value of both the mono and the stereo registers is 8000h (1000 0000 0000 0000), which corresponds to 0dB gain with mute on.

MUTE	MX4...MX0	FUNCTION
0	0 0000	0dB attenuation
0	0 0001	1.5dB attenuation
0	1 1111	46.5dB attenuation
1	x xxxx	$\infty$ dB attenuation

Table 4 Volume Register Function

**MASTER TONE CONTROL REGISTERS (INDEX 08h)**

Optional register for support of tone controls (bass and treble). The WM9708 does not support bass and treble and writing to this register will have no effect, reading will result in all zeros.

**PC BEEP REGISTER (INDEX 0Ah)**

This controls the level for the PC-beep input. Each step corresponds to approximately 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at  $-\infty$ dB.

WM9708 defaults to the PC-beep path being muted, except during reset when the path is open, so an external speaker should be provided within the PC to alert the user to power on self-test problems.

MUTE	PV3...PV0	FUNCTION
0	0000	0dB attenuation
0	1111	45dB attenuation
1	xxxx	$\infty$ dB attenuation

Table 5 PC-beep Register Function

**ANALOGUE MIXER INPUT GAIN REGISTERS (INDEX 0Ch - 18h AND 72h)**

This controls the gain/attenuation for each of the analogue inputs and mixer PGA. Each step corresponds to approximately 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at  $-\infty$ dB.

**REGISTER 0Eh (MIC VOLUME REGISTER)**

This has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on. The default value is 8008h, which corresponds to 0dB gain with mute on.

The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0dB gain with mute on.

MUTE	GX4...GX0	FUNCTION
0	00000	+12dB gain
0	01000	0dB gain
0	11111	-34.5dB gain
1	xxxxx	$-\infty$ dB gain

Table 6 Mixer Gain Control Register Function

**RECORD SELECT CONTROL REGISTER (INDEX 1Ah)**

Used to select the record source independently for right and left (see Table 7). The default value is 0000h, which corresponds to Mic in.

SR2 TO SR0	RIGHT RECORD SOURCE	SL2 TO SL0	LEFT RECORD SOURCE
0	Mic	0	Mic
1	CD in (R)	1	CD in (L)
2	Not supported	2	Not supported
3	Not supported	3	Not supported
4	Line in (R)	4	Line in (L)
5	Stereo mix (R)	5	Stereo mix (L)
6	Mono mix	6	Mono mix
7	Phone	7	Phone

Table 7 Record Select Register Function

**RECORD GAIN REGISTERS (INDEX 1Ch)**

1Ch is for the stereo input. Each step corresponds to 1.5dB. 22.5dB corresponds to 0F0Fh. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at  $-\infty$ dB.

The default value is 8000h, which corresponds to 0dB gain with mute on.

MUTE	GX3...GX0	FUNCTION
0	1111	+22.5dB gain
0	0000	0dB gain
1	xxxxx	$-\infty$ dB gain

Table 8 Record Gain Register Function

**GENERAL PURPOSE REGISTER (INDEX 20h)**

This register is used to control several miscellaneous functions of the WM9708.

Below is a summary of each bit and its function. Only the MIX, MS and LPBK bits are supported by the WM9708. The MS bit controls the Mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements. The function default value is 8000h which is all off.

BIT	FUNCTION	WM9708 SUPPORT
POP	PCM out path and mute	Yes
ST	Simulated stereo enhancement, on/off 1 = on	No
3D	3D stereo enhancement on/off, 1 = on	No
LD	Loudness (bass boost) on/off, 1 = on	No
LLBK	Local loop back - for modem, line codec	No
RLBK	Remote loop back - for modem, line codec	No
MIX	Mono output select 0 = Mix, 1 = Mic	Yes
MS	Mic select 0 = Mic1, 1 = Mic2	Yes
LPBK	ADC/DAC loopback mode	Yes

Table 9 General Purpose Register Function

**POWERDOWN CONTROL/STATUS REGISTER (INDEX 26h)**

This read/write register is used to program Powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a 1 indicating that the subsection is *ready*. *Ready* is defined as the subsection able to perform in its nominal state. When this register is written the bit values that come in on AC-link will have no effect on read only bits 0 to 7.

When the AC-link Codec Ready indicator bit (SDATAIN slot 0, bit 15) is a 1 it indicates that the AC-link and the WM9708 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

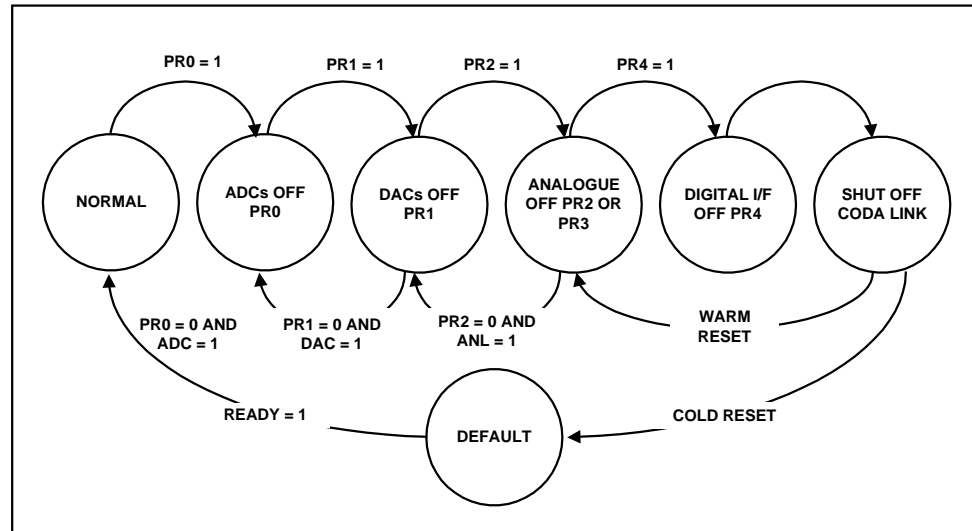
READ BIT	FUNCTION
REF	VREFs up to nominal level
ANL	Analogue mixers, etc ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

**Table 10 Powerdown Status Register Function**

The powerdown modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADCs and DACs only. PR6 is not supported by the WM9708.

WRITE BIT	FUNCTION
PR0	PCM in ADCs and input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analogue mixer Powerdown (VREF still on)
PR3	Analogue mixer Powerdown (VREF off)
PR4	Digital interface (AC-link) Powerdown (external clock off)
PR5	Internal clock disable
PR6	HP amp Powerdown – not supported
EAPD	External amplifier Powerdown

**Table 11 Powerdown Control Register Function**



**Figure 13 An Example of the WM9708 Powerdown/Powerup Flow**

Figure 13 illustrates one example procedure to do a complete Powerdown of the WM9708. From normal operation sequential writes to the Powerdown Register are performed to Powerdown the WM9708 a piece at a time. After everything has been shut off (PR0 to PR3 set), a final write (of PR4) can be executed to shut down the WM9708's digital interface (AC-link).

The part will remain in sleep mode with all its registers holding their static values. To wake up the WM9708, the AC'97 controller will send a pulse on the sync line issuing a warm reset. This will restart the WM9708's digital interface (resetting PR4 to 0). The WM9708 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers, as a cold reset will set them to their default states. When a section is powered back on, the Powerdown Control/Status Register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

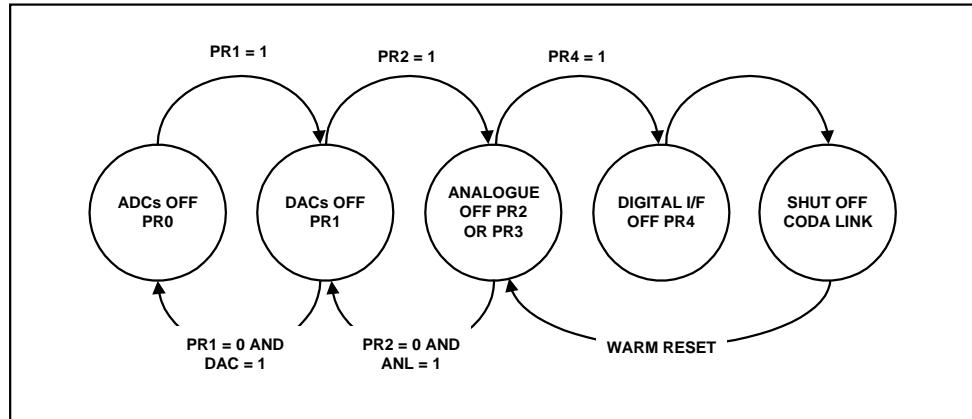


Figure 14 The WM9708 Powerdown/Flow with Analogue Still Alive

Figure 14 illustrates a state when all the mixers will work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINEIN source) through WM9708 to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analogue mixer is never shut down.

**POWERDOWN CONTROL/STATUS REGISTER (INDEX 26h)**

Note that in order to go into ultimate low power mode, PR4 and PR5 are required to be set which turns off the oscillator circuit. Asserting SYNC resets the PR4 and PR5 bit and re-starts the oscillator in the same was as the AC link is restarted.

**REVISION 2.1 REGISTERS (INDEX 28h TO 58h)**

These registers are specified as to use in Revision 2.1 of the AC'97 specification and have the following functions on the WM9708:

**REGISTER 28h – EXTENDED AUDIO ID**

The Extended Audio ID register is a read only register that identifies which extended audio features are supported (in addition to the original AC'97 features identified by reading the reset register at index 00h). A non zero value indicates the feature is supported.

DATA BIT	FUNCTION	ANY MODE
VRA	Variable rate audio support	1
DRA	Double rate audio support	0
VRM	Variable rate Mic ADC support	0
CDAC	Centre DAC support	0
SDAC	Surround DAC support	0
LDAC	LFE DAC support	0
AMAP	Slot to front DAC mapping support	0
ID1	Codec configuration – fixed in 9707	0
ID0	Not supported	Not supported

Table 12 Extended Audio ID Register

**REGISTER 2Ah – EXTENDED AUDIO STATUS AND CONTROL REGISTER**

The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

DATA BIT	FUNCTION	READ/WRITE	WM9708 SUPPORT
VRA	Enables variable rate audio mode	Read/write	Yes
DRA	Enable double rate audio mode	Read/write	No
VRM	Enables variable rate Mic ADC	Read/write	No
CDAC	Indicates centre DAC ready	Read	No
SDAC	Indicates surround DAC ready	Read	No
LDAC	Indicates LFE DAC ready	Read	No
MADC	Indicates Mic ADC ready	Read	No
PRI	Set to turn off centre DAC	Read/write	No
PRJ	Set to turn off surround DACs	Read/write	No
PRK	Set to turn off LFE DACs	Read/write	No
PRL	Set to turn off Mic ADC	Read/write	No

**Table 13 Extended Audio Status and Control Register**

**REGISTER 2Ch TO 32h – AUDIO SAMPLE RATE CONTROL REGISTERS**

These registers are read/write registers that are written to, to select alternative sample rates for the audio PCM converters. Default is the 48ks/s rate. Note that only Revision 2.1 recommended rates are supported by the WM9708, selection of any other unsupported rates will cause the rate to default to the nearest supported rate, and the supported rate value to be latched and so read back.

**REGISTERS 36h AND 38h – 6 CHANNEL VOLUME CONTROL**

These read/write registers control the output volume of the optional four PCM channels. (not supported by the WM9708)

**VENDOR RESERVED REGISTERS (INDEX 5Ah - 7Ah)**

These registers are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC '97 component.

**VENDOR SPECIFIC REGISTER (INDEX 5Ch)**

The WM9708 can be programmed to automute the DACs. By setting the mute bit, the WM9708 will mute the DACs when it detects a continuous sequence of 1024 zeros.

**VENDOR SPECIFIC GAIN CONTROL REGISTERS – (INDEX 72h)**

This register controls the gain and mute functions applied to the mixer path. This PGA is not accommodated in the Intel specification, but is required in order to allow the option of simultaneous recording of the mixer output and playback of DAC signals. The function is as per the other mixer PGA's. However, the default value of the register is not-muted. If it is not used it will be transparent to the user.

**VENDOR ID REGISTERS (INDEX 7Ch TO 7Eh)**

This register is for specific vendor identification if so desired. The ID method is Microsoft's Plug and Play Vendor ID code. The first character of that ID is F7 to F0, the second character S7 to S0, and the third T7 to T0. These three characters are ASCII encoded. The REV7 to REV0 field is for the Vendor Revision number. In the WM9708 the vendor ID is set to WML3.

Wolfson is a registered Microsoft Plug and Play vendor.

**VENDOR ID REGISTERS (INDEX 74h)**

This register describes how data is mapped to the AC'97 DACs. Register 74h can be used to change the incoming DAC data slots that are used by the on-board DACs. This allows software control of multiple codecs. If used it is recommended that the ID is configured before any other registers and before the data is applied to the system.



SURROUND SOUND DSS1, DSS0	PCM OUT LEFT	PCM OUT RIGHT
00	3	4
01	7	8
1X	6	9

**Table 14 Vendor ID Registers - Reg 74 [1:0]**

This allows the user to connect multiple codecs to a host controller using a single AC-link interface.

The volume control register is still 02h and the rate register is 2Ch. The ID pins have no effect on this mapping.

## SERIAL INTERFACE REGISTER MAP

The following table shows the function and address of the various control bits that are loaded through the serial interface during write operations.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	efault	
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6150h	
02h	Master volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h	
04h	LNLVL volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h	
06h	Master volume mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h	
0Ah	PCBEEP volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV2	PV0	X	8000h	
0Eh	Mic volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h	
10h	Line in volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h	
12h	CD volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h	
18h	PCM out volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h	
1Ah	Rec select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h	
1Ch	Rec gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h	
20h	General purpose	POP	ST	3D	ID	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h	
26h	Power/down control status	APD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh	
28h	Ext'd audio ID	ID1	ID0	X	X	X	X	Amap	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	1001h	
2Ah	Ext'd audio stat/ctrl	X	PRL	PRK	PRJ	PRI	X	Madc	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	0000h	
2Ch	Front DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h	
32h	Audio ADC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h	
5Ch	Vendor specific	REVISION					X	X	X	X	X	X	X	X	X	X	X	AME	1000h
72h	Front mixer volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	0808h	
74h	Surround sound	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DSS1	DSS0	0000h	
7Ah	Vendor reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h	
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	574Dh	
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0	4C03h	

**Table 15 Serial Interface Register Map Description****Note:**

All unused bits should have zeros written to them and will return the same when read.

RECOMMENDED EXTERNAL COMPONENTS

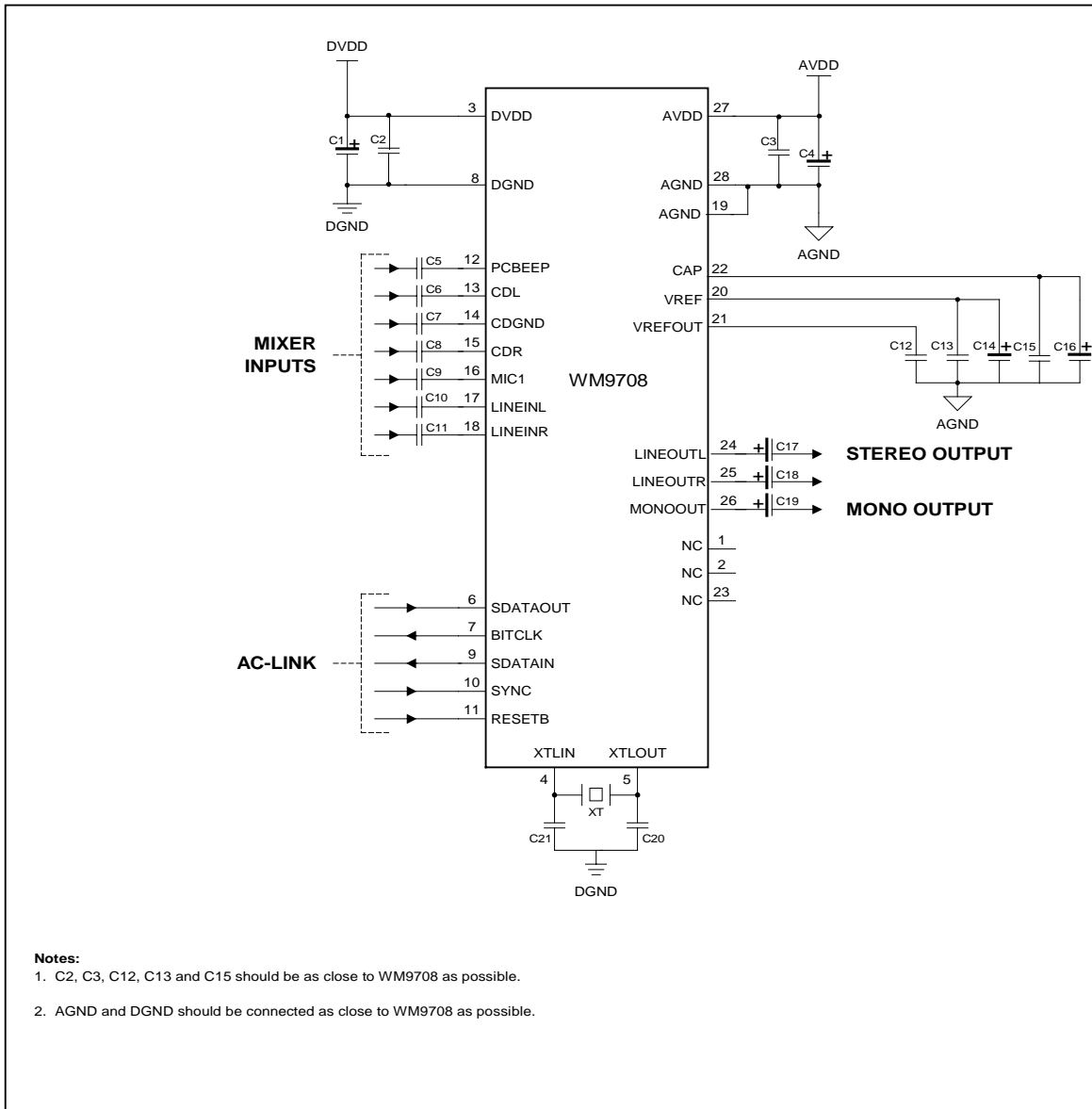


Figure 15 External Components Diagram

**RECOMMENDED EXTERNAL COMPONENTS VALUES**

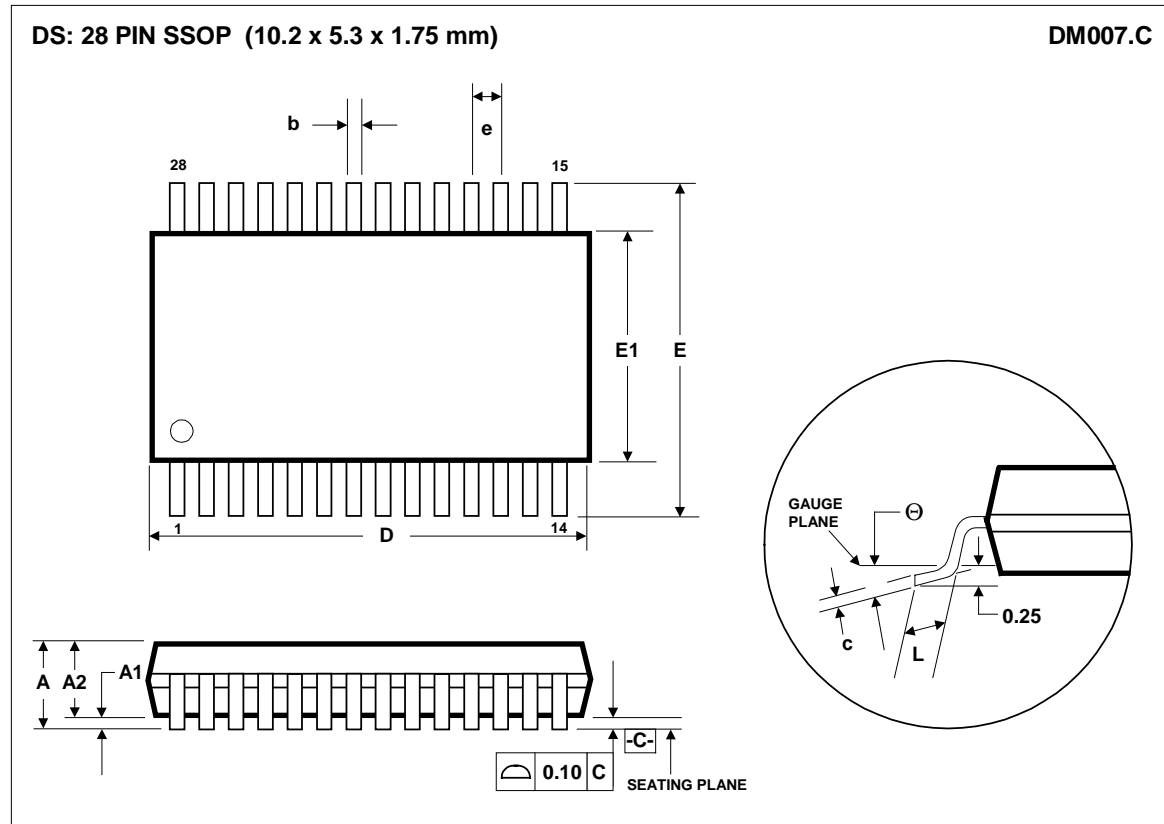
COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 to C4	10nF	De-coupling for DVDD and AVDD
C5 to C17	470nF	AC coupling capacitors for setting DC level of analogue inputs to VCAP1. Value chosen to give corner frequency below 20Hz for min 10K input impedance.
C18	1 $\mu$ F	Reference de-coupling capacitors for ADC, DAC, Mixer and CAP2 references. Ceramic type or similar.
C19	0.1 $\mu$ F	
C20	10 $\mu$ F	
C21	0.1 $\mu$ F	
C22	10 $\mu$ F	
C23	100nF	
C24	47nF	3D high pass filter. This value sets nominal 1kHz.
C25 to C29	10 $\mu$ F	Output AC coupling caps to remove VREF DC level from outputs.
C30 and C31	22pF	Optional capacitors for better crystal frequency stability.
XT	24.576 MHz	AC'97 master clock frequency. A bias resistor is not required, but if connected will not affect operation if value is large (above 1M $\Omega$ ).

**Table 16 External Component Values****RECOMMENDATIONS FOR 3.3V OPERATION**

The device's performance with AVDD = 3.3V is shown in Electrical Characteristics.

In 3.3V analogue operation, mid-rail reference scales to 1.5V. All ADC and DAC references are 3/5<sup>th</sup>s of their nominal 5V value. Input and output signals that are 1V<sub>rms</sub> in 5V applications, scale to 660mV<sub>rms</sub> in 3.3V applications. If 1V<sub>rms</sub> output is required, the mixer gain adjust PGAs need to be increased by 3 times 1.5dB steps.

PACKAGE DIMENSIONS



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
<b>A</b>	-----	-----	2.0
<b>A<sub>1</sub></b>	0.05	-----	-----
<b>A<sub>2</sub></b>	1.62	1.75	1.85
<b>b</b>	0.22	-----	0.38
<b>c</b>	0.09	-----	0.25
<b>D</b>	9.90	10.20	10.50
<b>e</b>	0.65 BSC		
<b>E</b>	7.40	7.80	8.20
<b>E<sub>1</sub></b>	5.00	5.30	5.60
<b>L</b>	0.55	0.75	0.95
<b>θ</b>	0°	4°	8°
<b>REF:</b>	JEDEC.95, MO-150		

- NOTES:  
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.  
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.  
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.  
 D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.