SONY

ILX128MA

5350-pixel × 6-line CCD Linear Sensor (Color)

Description

The ILX128MA is a reduction type CCD linear sensor developed for color image scanner, and has shutter function per each color. This sensor reads A3-size documents at a density of pseudo 800DPI, and reads A4-size at a density of pseudo 1200DPI.

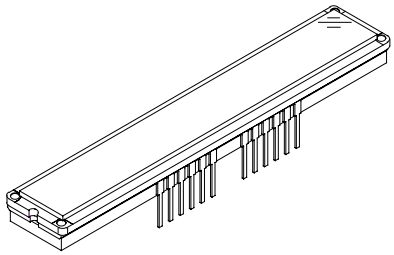
Features

- Number of effective pixels: 32100 pixels (5350 pixels × 6)
- Pixel size: 6µm × 8µm (8µm pitch)
- Distance between line: 48µm (6 lines: Rsub – Rmain, Rmain – Gsub, Gsub – Gmain, Gmain – Bsub, Bsub – Bmain)
- Single-sided readout
- Shutter function
- Ultra-high sensitivity/Ultra-low lag
- Supply voltage: Single 12V power supply
- Input clock pulse: CMOS 5V drive
- Number of output: 3 (R, G, B)
- Package: 24-pin Plastic-DIP

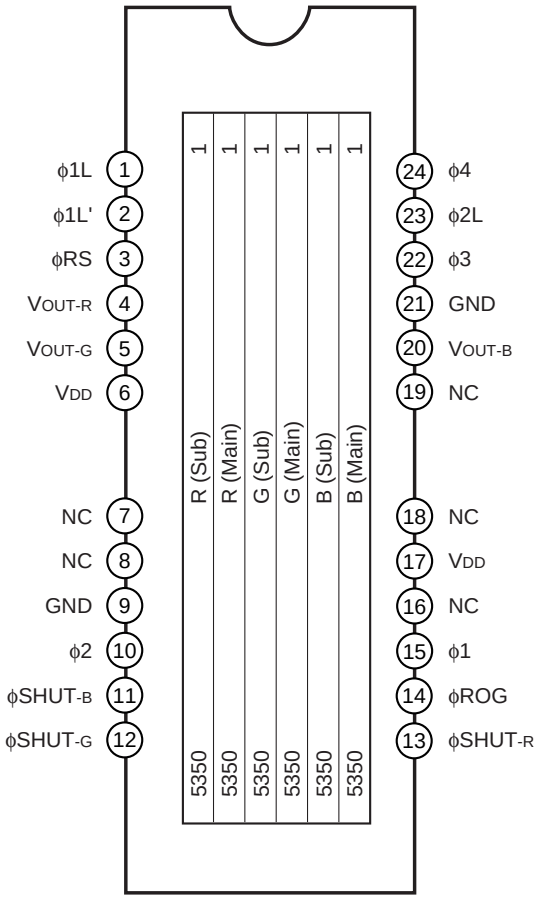
Absolute Maximum Ratings

• Supply voltage	V_{DD}	15	V
• Input clock voltage		7	V
• Operating temperature		–10 to +55	°C
• Storage temperature		–30 to +80	°C

24 pin DIP (Plastic)

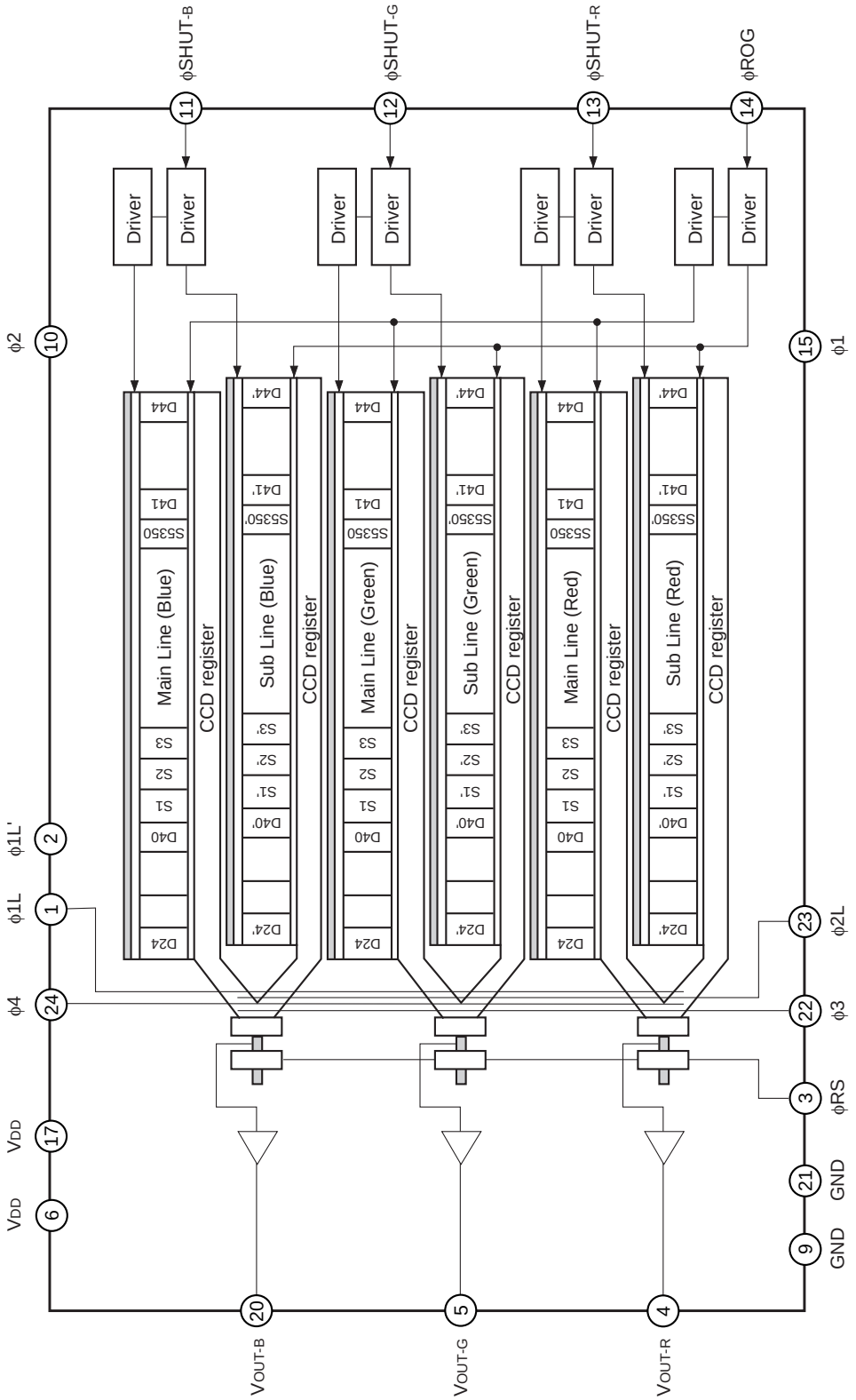


Pin Configuration (Top View)



E00462-PS

Block Diagram



Note) D24 and D24' are the start pixels for the optical black of Main Line and Sub Line. (These are not pixels immediately before multiplex.)

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	φ1L	Clock pulse input	13	φSHUT-R	Clock pulse input
2	φ1L'	Clock pulse input	14	φROG	Clock pulse input
3	φRS	Clock pulse input	15	φ1	Clock pulse input
4	V_{OUT-R}	Signal output (red)	16	NC	NC*
5	V_{OUT-G}	Signal output (green)	17	V_{DD}	12V power supply
6	V_{DD}	12V power supply	18	NC	NC
7	NC	NC	19	NC	NC
8	NC	NC	20	V_{OUT-B}	Signal output (blue)
9	GND	GND	21	GND	GND
10	φ2	Clock pulse input	22	φ3	Clock pulse input
11	φSHUT-B	Clock pulse input	23	φ2L	Clock pulse input
12	φSHUT-G	Clock pulse input	24	φ4	Clock pulse input

* Connecting to GND is recommended.

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	11.4	12	12.6	V

Input Pin Capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of φ1, φ2	$C_{\phi 1}$, $C_{\phi 2}$	—	1530	—	pF
Input capacity of φ1L, φ1L', φ2L	$C_{\phi 1L}$, $C_{\phi 1L'}$, $C_{\phi 2L}$	—	20	—	pF
Input capacity of φ3, φ4	$C_{\phi 3}$, $C_{\phi 4}$	—	20	—	pF
Input capacity of φRS	$C_{\phi RS}$	—	20	—	pF
Input capacity of φROG	$C_{\phi ROG}$	—	10	—	pF
Input capacity of φSHUT*1	$C_{\phi SHUT}$	—	10	—	pF

*1 φSHUT represents φSHUT-R, φSHUT-G and φSHUT-B.

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
ϕ1, ϕ2, ϕ1L, ϕ1L', ϕ2L	$f\phi_1$, $f\phi_2$, $f\phi_{1L}$, $f\phi_{1L'}$, $f\phi_{2L}$	—	1	3	MHz
ϕ3, ϕ4	$f\phi_3$, $f\phi_4$	—	2	6	MHz
ϕRS	$f\phi_{RS}$	—	2	6	MHz

Input Clock Voltage Condition

Item		Min.	Typ.	Max.	Unit
ϕ1L, ϕ1L', ϕ2L, ϕ3, ϕ4	High level	4.75	5.0	5.25	V
	Low level	0	—	0.1	V
ϕ1, ϕ2, ϕRS, ϕROG, ϕSHUT	High leve	4.75	5.0	5.25	V
	Low level	0	—	0.5	V

Electrooptical Characteristics (Note 1) (Ta = 25°C, V_{DD} = 12V, $f\phi_{RS}$ = 2MHz, Input clock = 5Vp-p, Light source = 3200K, IR cut filter CM-500S (t = 1mm))

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	1.33	1.9	2.47	V/(lx · s)	Note 2
	Green	R_G	3.01	4.3	5.59		
	Blue	R_B	1.82	2.6	3.38		
Sensitivity nonuniformity		PRNU	—	4	15	%	Note 3
Adjacent pixel difference		PDF	—	4	15	%	Note 4
Saturation output voltage		V_{SAT}	2	3	—	V	Note 5
Overflow exposure		OE	2 × SEmin	—	—		Note 6
Saturation exposure	Red	SE_R	0.8	1.6	—	lx · s	Note 7
	Green	SE_G	0.4	0.7	—		
	Blue	SE_B	0.6	1.2	—		
Dark voltage average		V_{DRK}	—	0.3	2.0	mV	Note 8
Dark signal nonuniformity		DSNU	—	1.5	5.0	mV	Note 9
Image lag		IL	—	0.02	—	%	Note 10
Current consumption		I_{VDD}	—	32	50	mA	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	250	—	Ω	—
Offset level		V_{OS}	4.7	6.2	7.7	V	Note 11
Offset level difference		ΔV_{OS}	—	40	200	mV	Note 12
Dynamic range		DR	1000	10000	—	—	Note 13

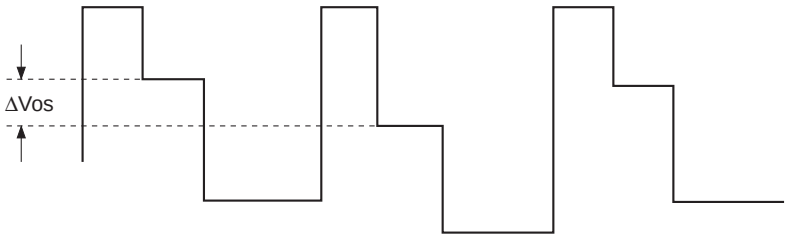
Note)

1. For each color, the black level of Main Line is defined as the average value of D24, D25 to D39, and the black level of Sub Line is defined as the average value of D24', D25' to D39'. The following electrooptical characteristics signal processing is performed.
2. For the sensitivity test light is applied with a uniform intensity of illumination.
3. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.
   V_{OUT} = 500mV (Typ.)

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

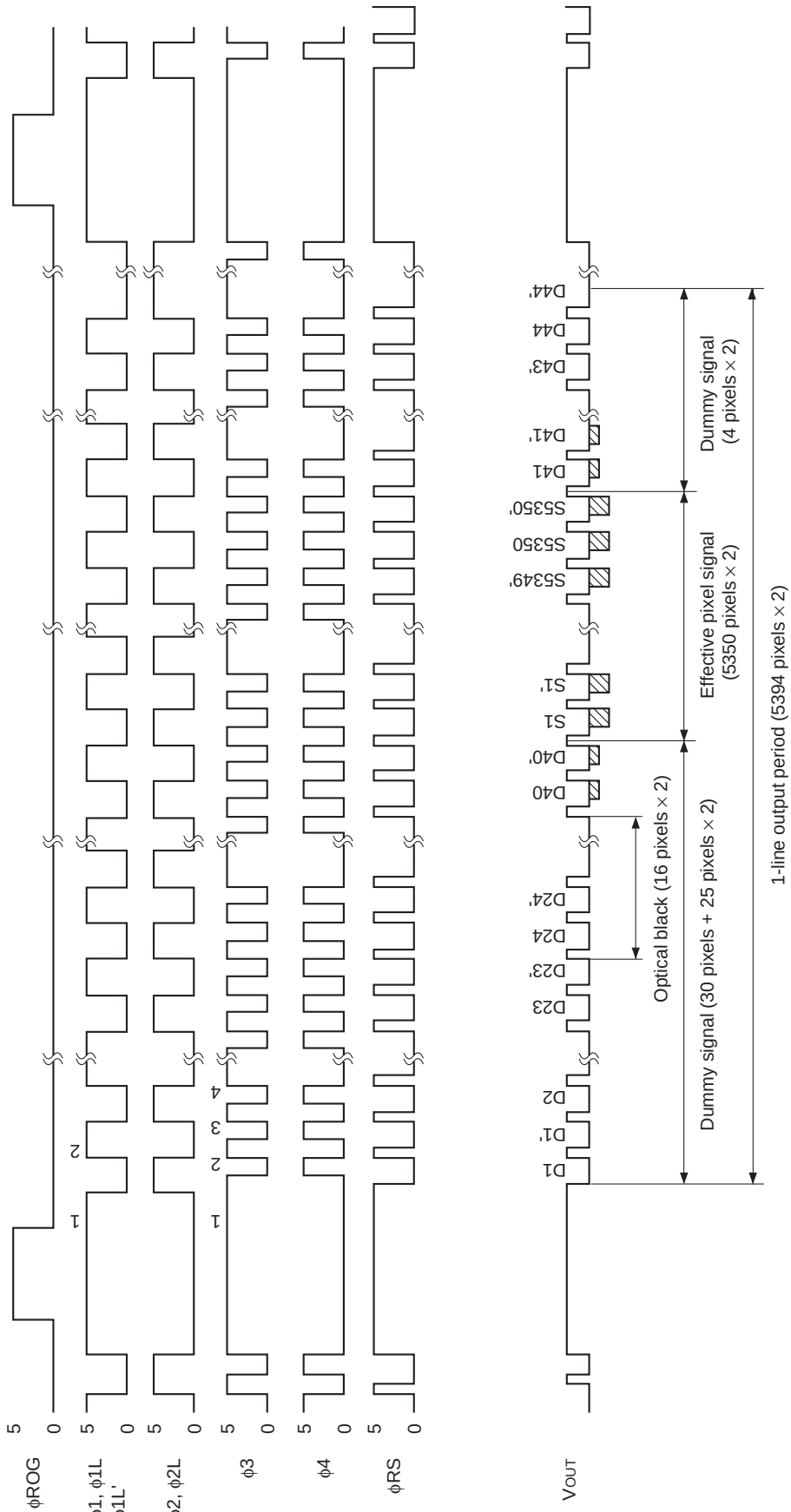
   Where the maximum output of the effective pixels is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
4. PDF = $(\Delta V_{MAX}/V_{AVE}) \times 100$ [%]
   Here, V_{AVE} is defined as the average output, and ΔV_{MAX}, the maximum value of ΔVi in the range of the following pixel.
   Red, green, blue pixel arrangement PDF is when i = 1 to 5349. However, the definition of ΔVi is as follows.
   $\Delta Vi = ABS \{V_{OUT}(i) - V_{OUT}(i + 1)\}$
   V_{OUT} (i) is signal output of an effective pixel (i pixel) and V_{OUT} (i + 1) is of the adjacent pixel (i + 1 pixel).

5. Specifies at the minimum value of the saturation output voltage.
6. SEmin is the exposure at the minimum value (2V) of the saturation output voltage.
7. Saturation exposure is defined as in the right figure. SE = V_{SAT}/R
8. For each color, Main Line is defined by the difference between the average value of D2 to D22 dummy signal during no incident light and of D24 to D40, S1 to S5350. Sub Line is defined by the difference between the average value of D2' to D22' dummy signal during no incident light and of D24' to D40', S1' to S5350'.
   Optical signal integration time τint stands at 10ms.
9. For each color, calculate the difference as follows; the maximum and minimum values of the dark output voltage of respective Main Line and Sub Line; the dark voltage average value of respective Main Line and Sub Line. Then, the highest value is defined as dark signal nonuniformity.
   Optical signal integration time τint stands at 10ms.
10. V_{OUT} = 500mV (Typ.)
11. Vos is defined as the output DC value when ϕRS is high.
12. For each color, the Main Line offset level of the optical black pixel is defined as Vos-main, the Sub Line offset level, Vos-sub. Then, the offset level difference is defined as indicated below.
    ΔV_{OS} = | V_{OS}-main – V_{OS}-sub |
    ϕ1L and ϕ1L' are set to the same clock input.



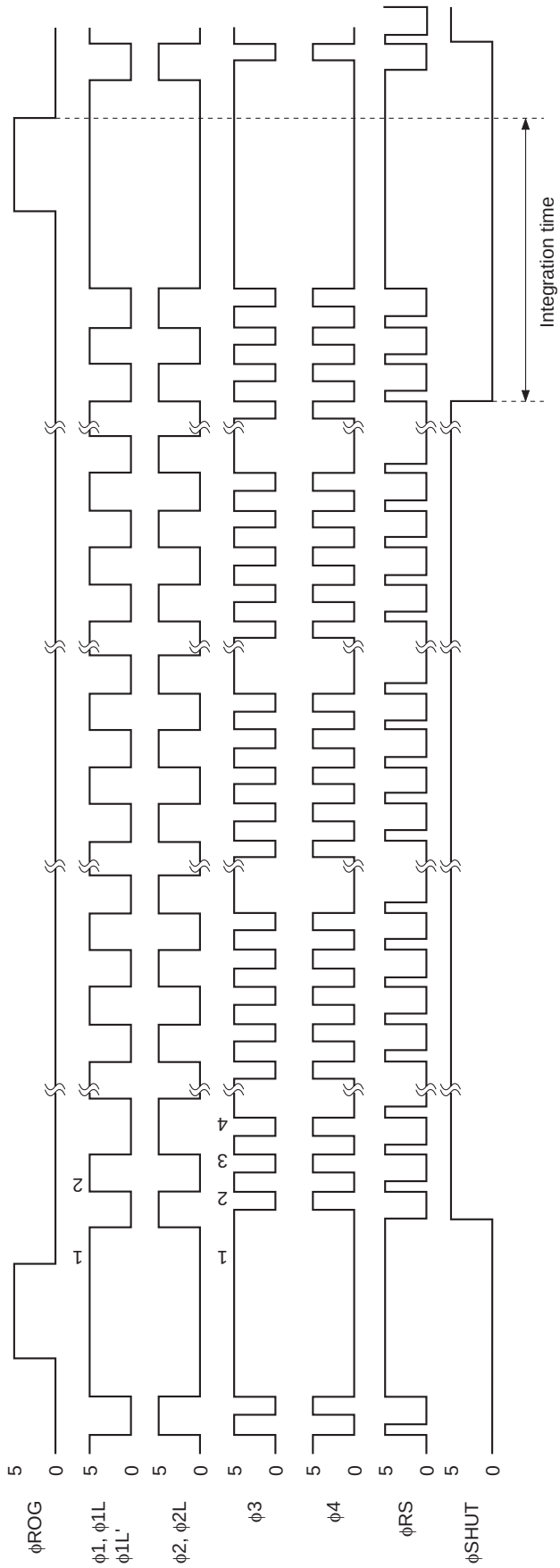
13. Dynamic range is defined as follows.
    DR = V_{SAT}/V_{DRK}
    When the optical signal integration time is shorter, the dynamic range gets wider because the optical signal integration time is in proportion to the dark voltage.

Clock Timing Chart 1



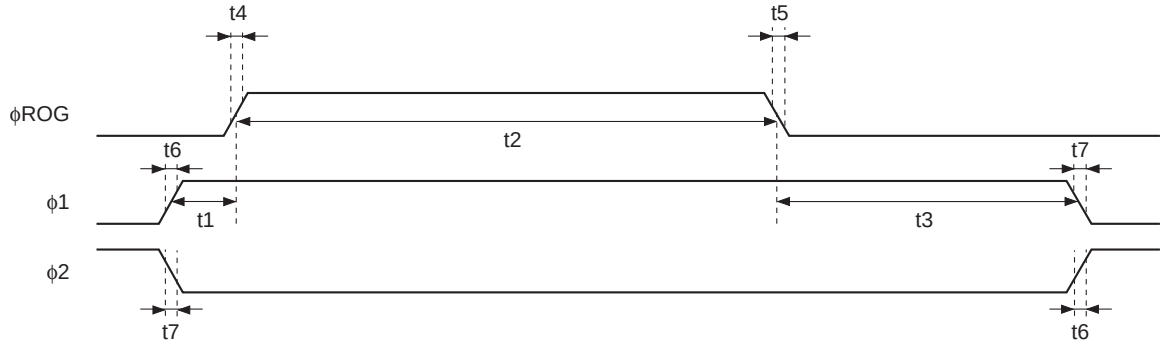
Note) The transfer pulse φ1, φ2, φ1L, φ1L' and φ2L must have more than 5394 cycles.
φ3 and φ4 must have more than 10788 cycles.

Clock Timing Chart 2 (shutter operation)

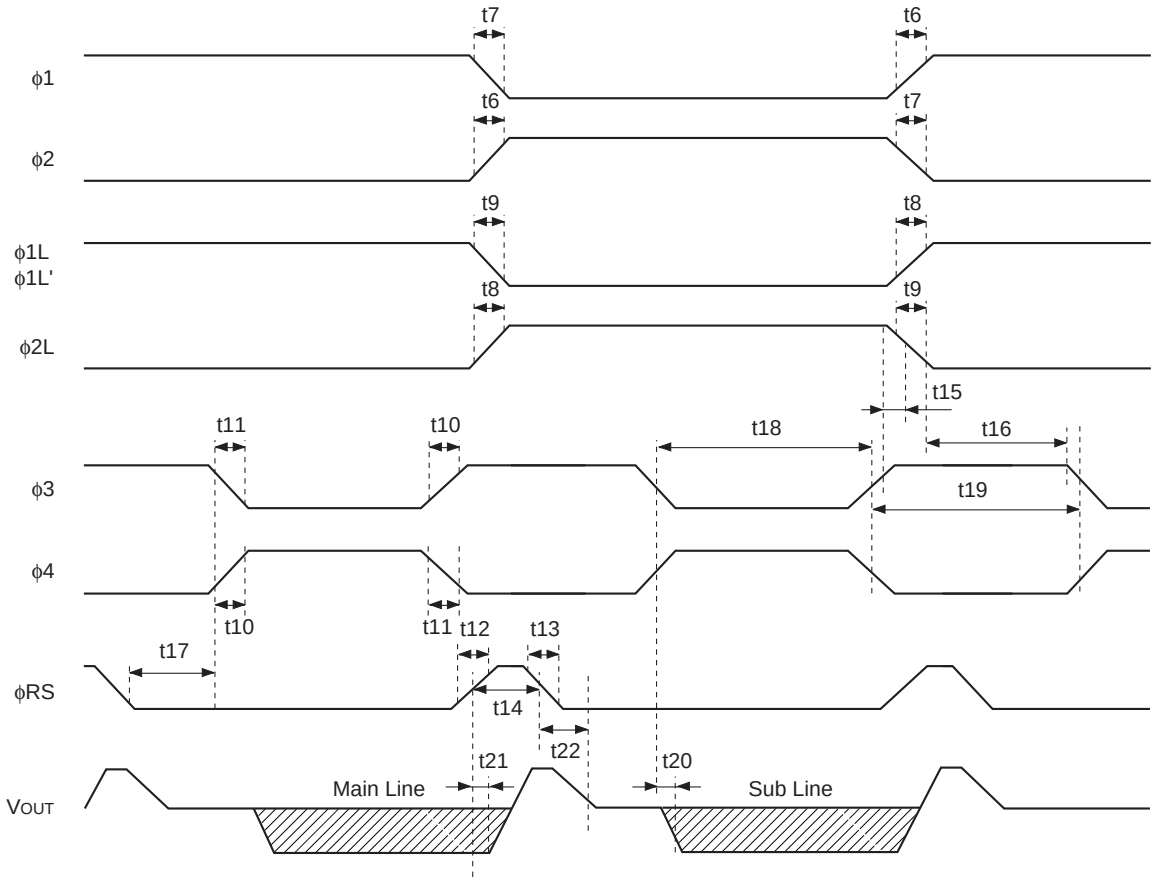


Note) Shutter pulse must not be high to low level or low to high level during effective pixel period.

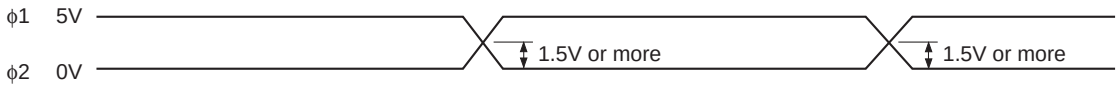
Clock Timing Chart 3



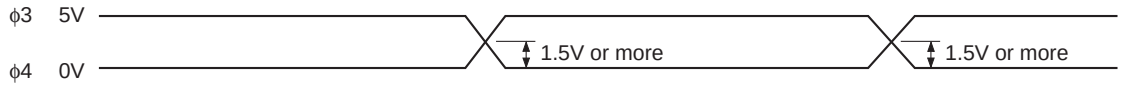
Clock Timing Chart 4



ϕ1 and ϕ2 Cross Point



ϕ3 and ϕ4 Cross Point



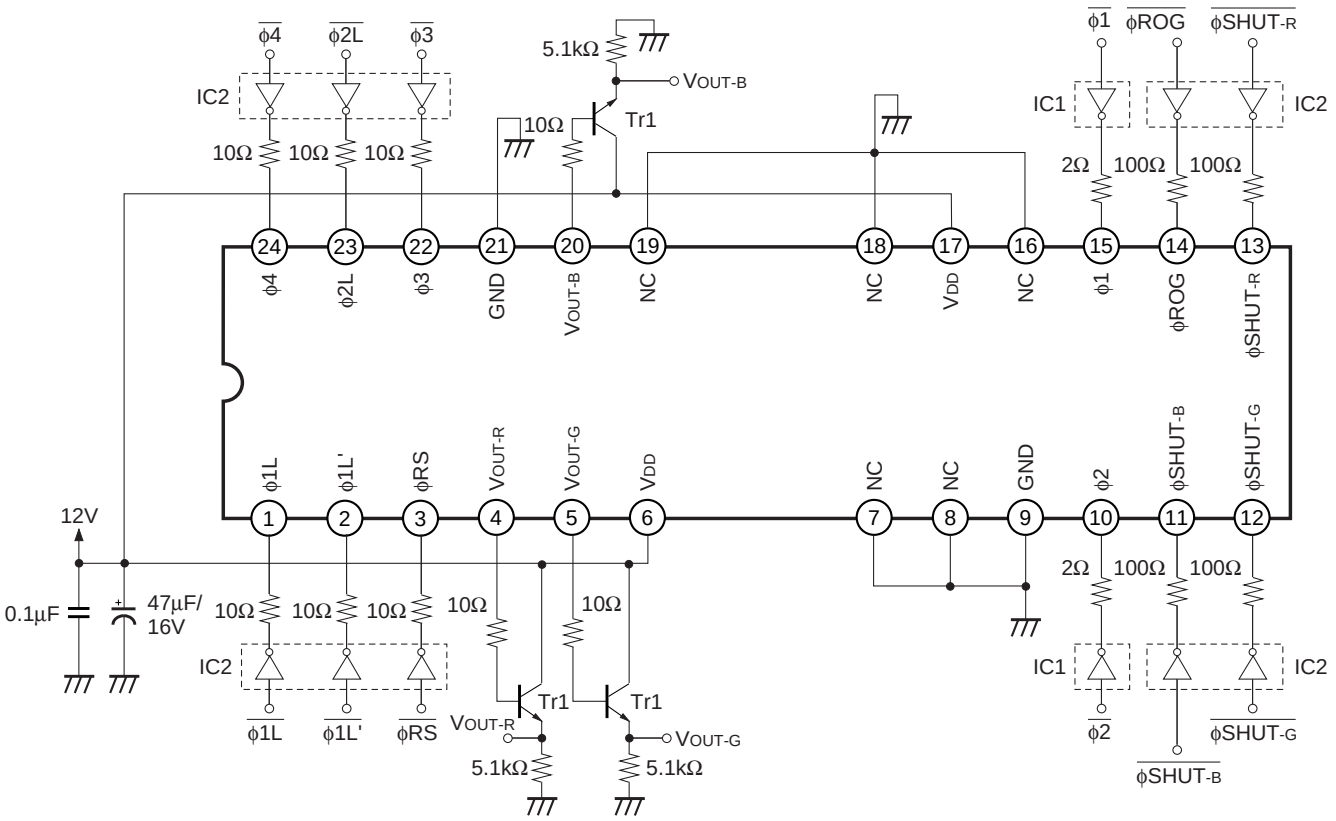
Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φ1 pulse timing	t1	50	100	—	ns
φROG pulse high level period	t2	1200	1500	—	ns
φROG, φ1 pulse timing	t3	1200	1500	—	ns
φROG pulse rise time	t4	0	5	10	ns
φROG pulse fall time	t5	0	5	10	ns
φ1 pulse rise/φ2 pulse fall time	t6	0	20	60	ns
φ1 pulse fall/φ2 pulse rise time	t7	0	20	60	ns
φ1L, φ1L' pulse rise/φ2L pulse fall time	t8	0	10	30*1	ns
φ1L, φ1L' pulse fall/φ2L pulse rise time	t9	0	10	30*1	ns
φ3 pulse rise/φ4 pulse fall time	t10	0	10	30*1	ns
φ3 pulse fall/φ4 pulse rise time	t11	0	10	30*1	ns
φRS pulse rise time	t12	0	10	30*1	ns
φRS pulse fall time	t13	0	10	30*1	ns
φRS pulse high level period	t14	20	250*1	—	ns
φ1L', φ2L – φ3, φ4 pulse timing 1	t15	35	40	—	ns
φ1L', φ2L – φ3, φ4 pulse timing 2	t16	35	210*1	—	ns
φRS, φ3 pulse timing	t17	50	125*1	—	ns
φ3, φ4 pulse low level period	t18	35	250	—	ns
	t19	35	250	—	ns
Signal output delay time	t20	—	35	—	ns
	t21	—	8	—	ns
	t22	—	35	—	ns

The recommended duty of φ1, φ2, φ1L, φ2L, φ3 and φ4 = 50%.

*1 These timing is the recommended condition under $f_{\phi RS}$ = 2MHz.

Application Circuit*1



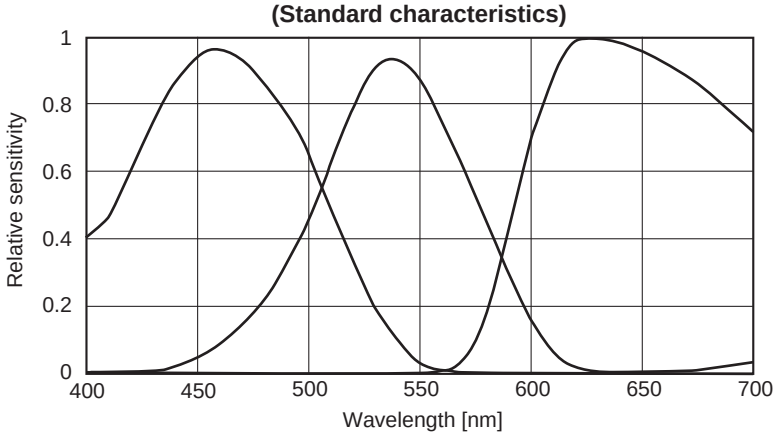
IC1: 74AC04
IC2: 74HC04
Tr1: 2SC2785

*1 Data rate $f_{\phi RS}$ = 2MHz

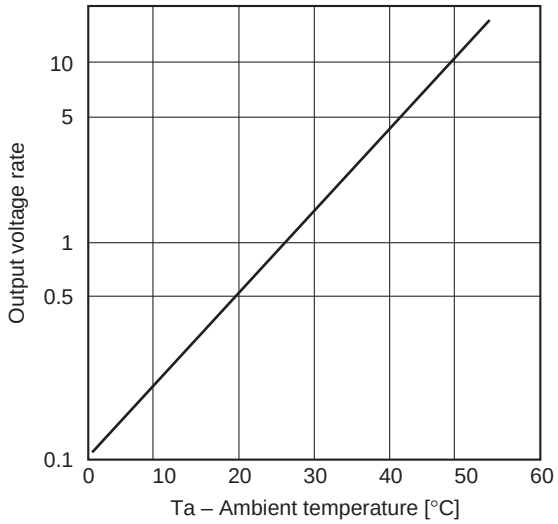
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD} = 12V, Ta = 25°C)

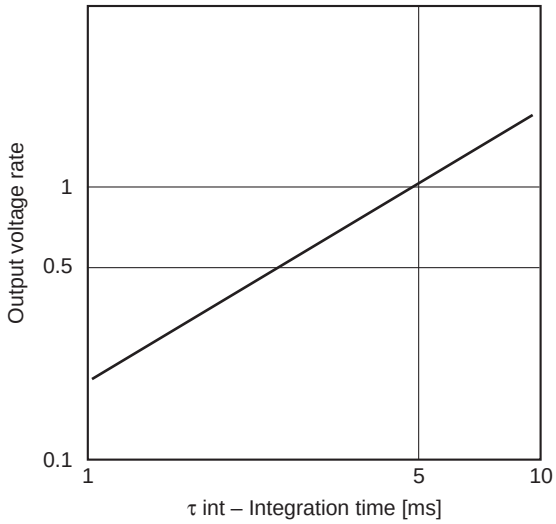
Spectral sensitivity characteristics (Standard characteristics)



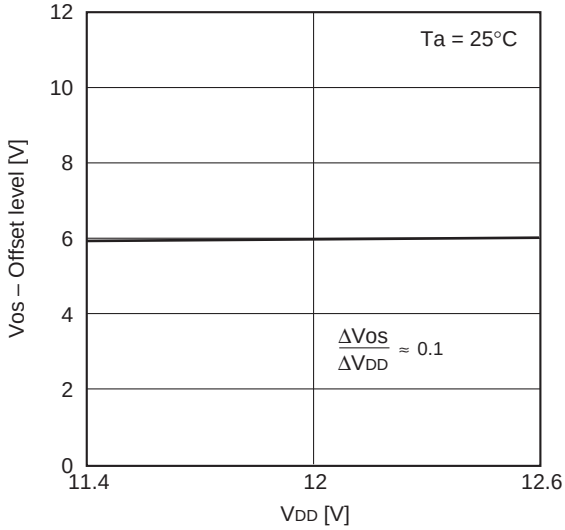
Dark signal output temperature characteristics (Standard characteristics)



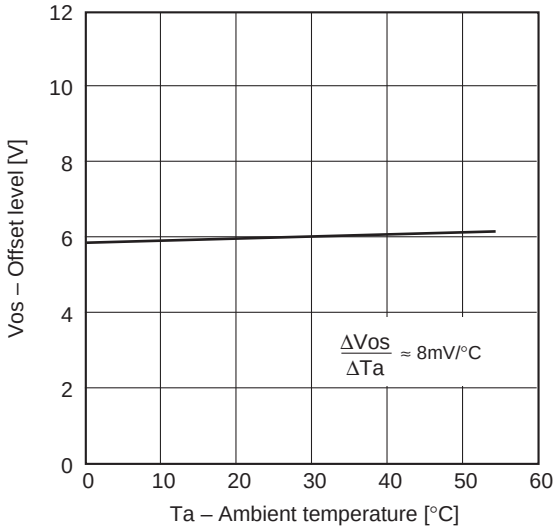
Integration time output voltage characteristics (Standard characteristics)



Offset level vs. V_{DD} characteristics (Standard characteristics)



Offset level vs. temperature characteristics (Standard characteristics)



Notes on Handling

1. Static charge prevention

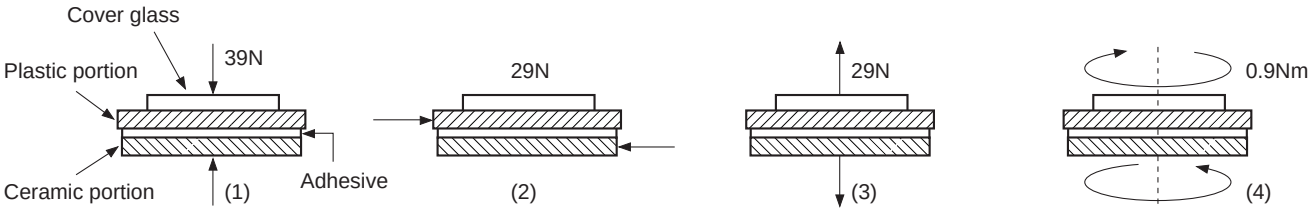
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

   a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Notes on Handling CCD Packages

   The following points should be observed when handling and installing plastic packages.

   a) Remain within the following limits when applying static load to the package.
      (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
      (2) Shearing strength: 29N/surface
      (3) Tensile strength: 29N/surface
      (4) Torsional strength: 0.9Nm



   b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
   c) Be aware that any of the following can cause the package to crack or dust to be generated.
      (1) Applying repetitive bending stress to the external leads.
      (2) Applying heat to the external leads for an extended period of time with soldering iron.
      (3) Rapid cooling or heating.
      (4) Prying the plastic portion and ceramic portion away at a support point of the adhesive layer.
      (5) Applying the metal a crash or a rub against the plastic portion.

   Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

   d) The notch of the plastic portion is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch or ceramic may overlap with the notch of the plastic portion.

3. Soldering

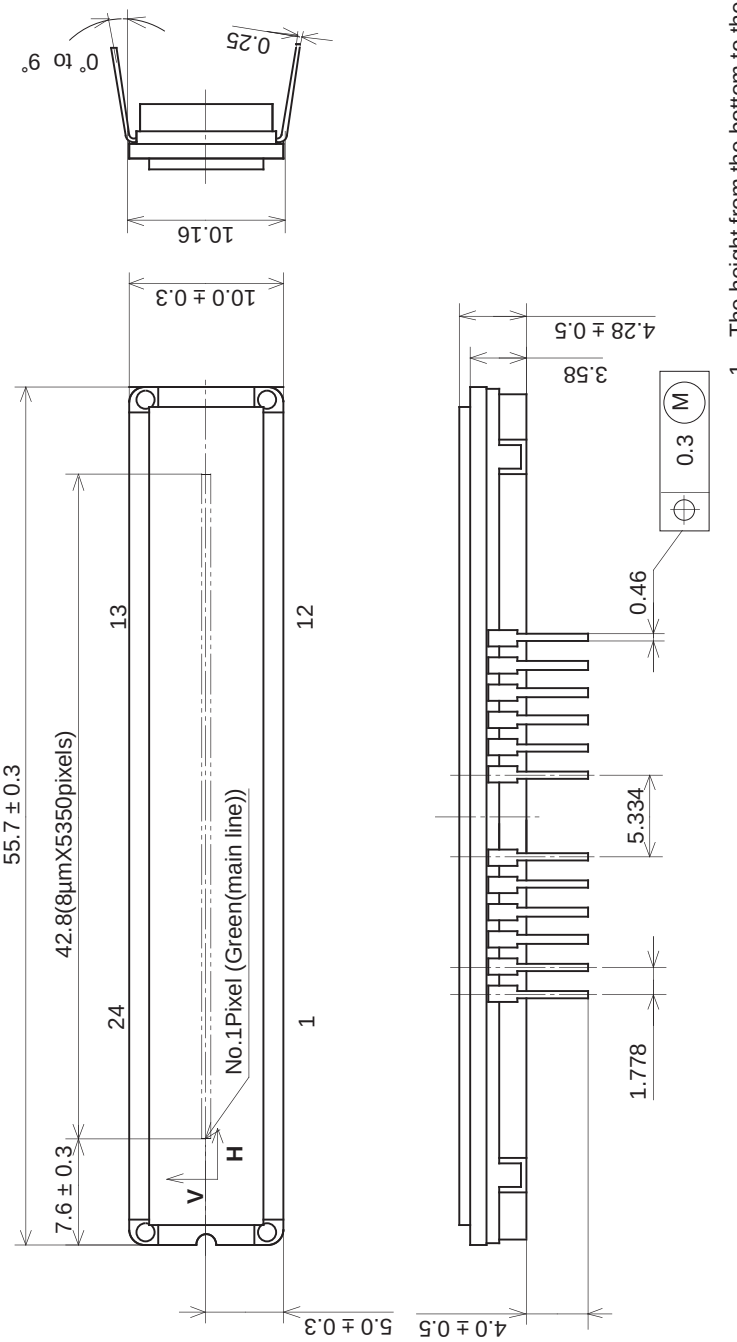
   a) Make sure the package temperature does not exceed 80°C.
   b) Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, ground the controller. For the temperature control system, use a zero-cross type.

4. Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch mirror surfaces by hand or have any object come in contact with mirror surfaces. Should dirt stick to a mirror surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the mirror surfaces are grease stained. Be careful not to scratch the mirror surfaces.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation on the mirror surfaces, preheat or precool when moving to a room with great temperature differences.

5. Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm



1. The height from the bottom to the sensor surface is 2.38 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic-Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42ALLOY
PACKAGE MASS	5.43g
DRAWING NUMBER	LS-B27(E)