CY62136CV30/33 MoBL®
CY62136CV MoBL®

2M (128K x 16) Static RAM

Features

- **Very high speed: 55 ns and 70 ns**
- **Voltage range:**
  - **CY62136CV30: 2.7V–3.3V**
  - **CY62136CV33: 3.0V–3.6V**
  - **CY62136CV: 2.7V–3.6V**
- **Pin-compatible with the CY62136V**
- **Ultra-low active power**
  - **Typical active current: 1.5 mA @ f = 1 MHz**
  - **Typical active current: 5.5 mA @ f = f_{max} (70-ns speed)**
- **Low standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball FBGA**

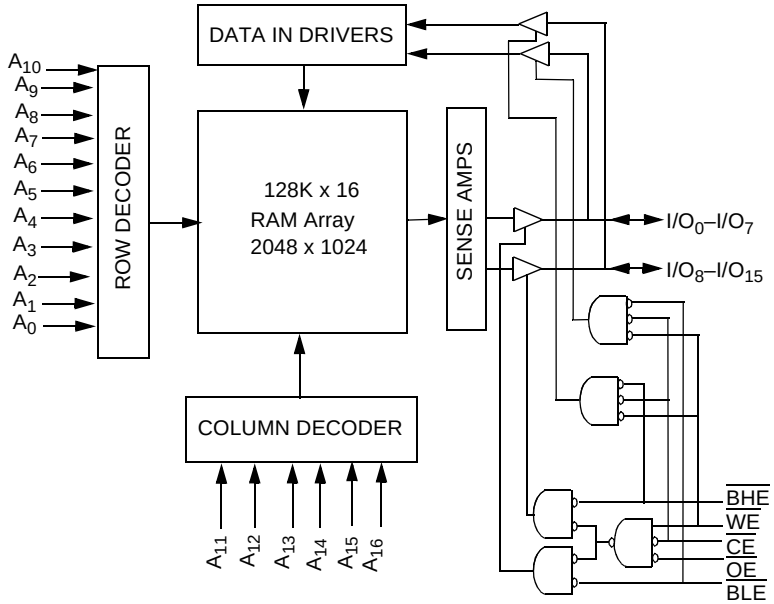
Functional Description[1]

The and CY62136CV are high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

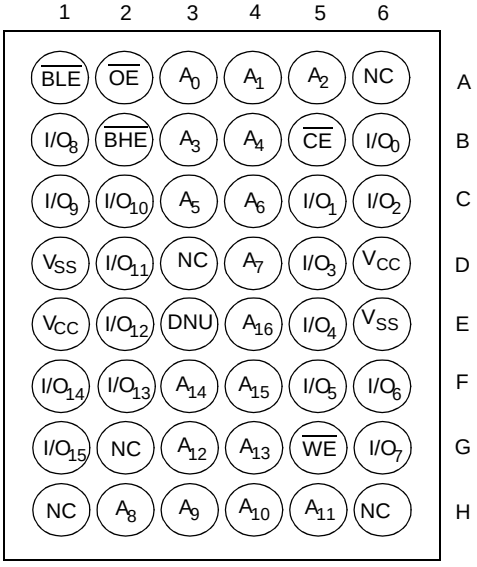
Logic Block Diagram



Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Pin Configuration[2, 3]

FBGA (Top View)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential –0.5V to V_{CCMAX} + 0.5V

DC Voltage Applied to Outputs in High-Z State[4].....–0.5V to V_{CC} + 0.3V

DC Input Voltage[4].....–0.5V to V_{CC} + 0.3V

Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62136CV30	Industrial	–40°C to +85°C	2.7V to 3.3V
CY62136CV33			3.0V to 3.6V
CY62136CV			2.7V to 3.6V

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating, I_{CC} (mA)				Standby, I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	$V_{CC(min.)}$	$V_{CC(typ.)}$[5]	$V_{CC(max.)}$		Typ.[5]	Max.	Typ.[5]	Max.	Typ.[5]	Max.
CY62136CV30LL	2.7	3.0	3.3	55	1.5	3	7	15	2	10
				70	1.5	3	5.5	12		
CY62136CV33LL	3.0	3.3	3.6	55	1.5	3	7	15	5	15
				70	1.5	3	5.5	12		
CY62136CVLL	2.7	3.3	3.6	70	1.5	3	5.5	12	5	15

Notes:
2. NC pins are not connected to the die.
3. E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
4. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62136CV30-55 Min.	CY62136CV30-55 Typ.[5]	CY62136CV30-55 Max.	CY62136CV30-70 Min.	CY62136CV30-70 Typ.[5]	CY62136CV30-70 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = 2.7V	2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 2.7V			0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2		V_{CC} + 0.3V	2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage			–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = 3.3V, I_{OUT} = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz			1.5	3		1.5	3	
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = f_{max} (Address and Data Only), f = 0 (OE, WE, BHE, and BLE)			2	10		2	10	µA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.3V								

Parameter	Description	Test Conditions		CY62136CV33-55 Min.	CY62136CV33-55 Typ.[5]	CY62136CV33-55 Max.	CY62136CV33-70 CY62136CV-70 Min.	CY62136CV33-70 CY62136CV-70 Typ.[5]	CY62136CV33-70 CY62136CV-70 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = 3.0V	2.4			2.4			V
			V_{CC} = 2.7V				2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 3.0V			0.4			0.4	V
			V_{CC} = 2.7V						0.4	V
V_{IH}	Input HIGH Voltage			2.2		V_{CC} + 0.3V	2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage			–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = 3.6V, I_{OUT} = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz			1.5	3		1.5	3	
I_{SB1}	Automatic CE Power-down Current —CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = f_{max} (Address and Data Only), f = 0 (OE, WE, BHE, and BLE)			5	15		5	15	µA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.6V								

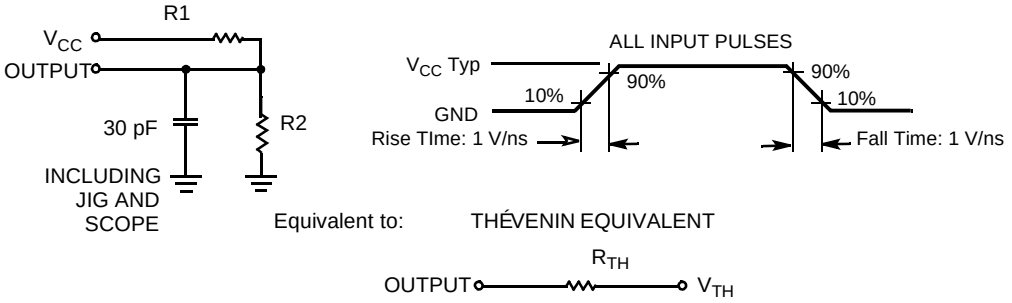
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[6]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[6]		16	°C/W

AC Test Loads and Waveforms

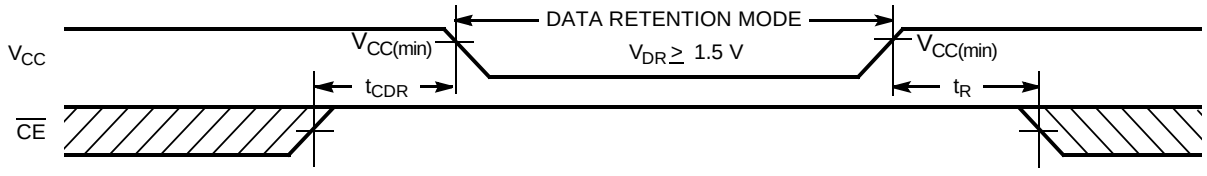


Parameters	3.0V	3.3V	Unit
R1	1105	1216	Ω
R2	1550	1374	Ω
R_{TH}	645	645	Ω
V_{TH}	1.75	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.[5]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5		V_{ccmax}	V
I_{CCDR}	Data Retention Current	V_{CC}= 1.5V $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	6	µA
t_{CDR}[6]	Chip Deselect to Data Retention Time		0			ns
t_R[7]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



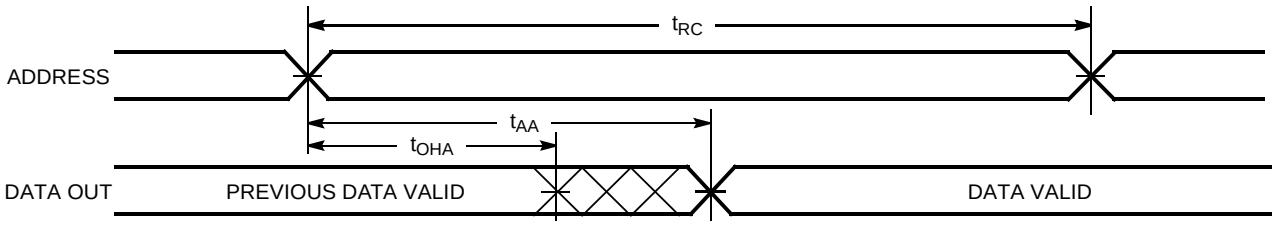
Notes:
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ > 100 µs or stable at $V_{CC(min.)}$ > 100 µs.

Switching Characteristics Over the Operating Range[8]

Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[9]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[9, 10]		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[9]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[9, 10]		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		55		70	ns
t_{DBE}	$\overline{BHE}$/$\overline{BLE}$ LOW to Data Valid		25		35	ns
t_{LZBE}	$\overline{BHE}$/$\overline{BLE}$ LOW to Low-Z[9]	5		5		ns
t_{HZBE}	$\overline{BHE}$/$\overline{BLE}$ HIGH to High-Z[9, 10]		20		25	ns
Write Cycle[11]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		45		ns
t_{BW}	$\overline{BHE}$/$\overline{BLE}$ Pulse Width	50		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[9, 10]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[9]	10		10		ns

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)[12, 13]

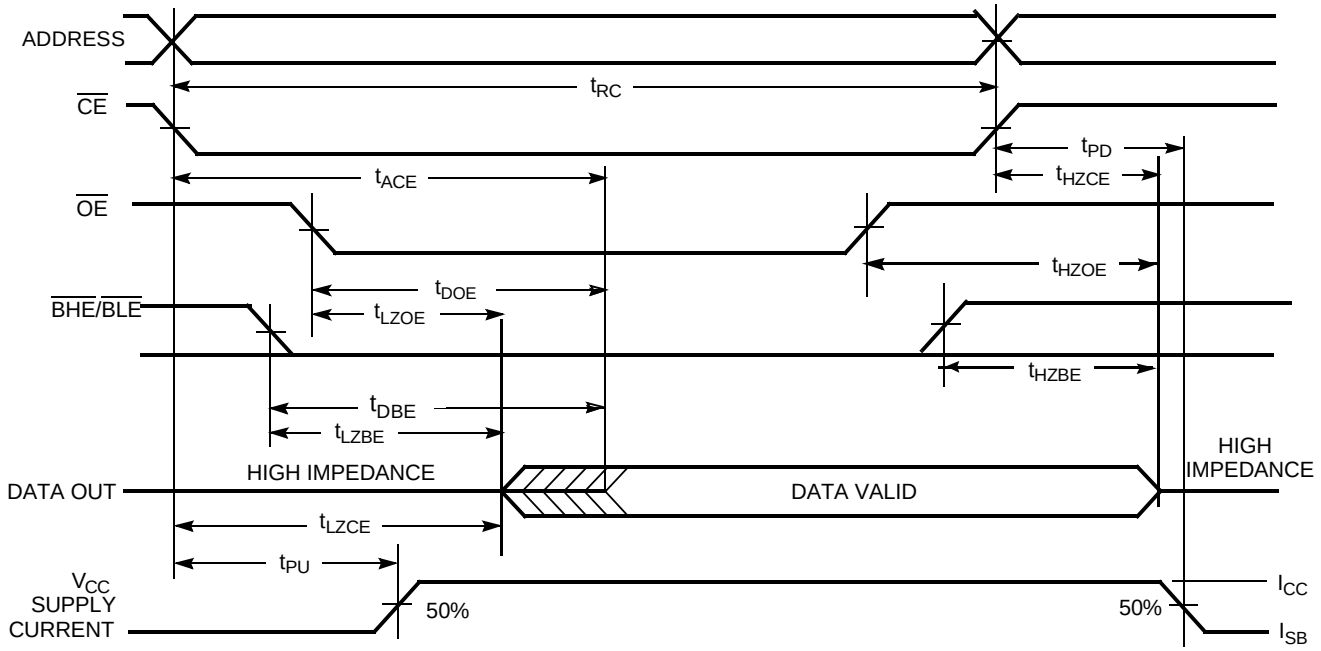


Notes:

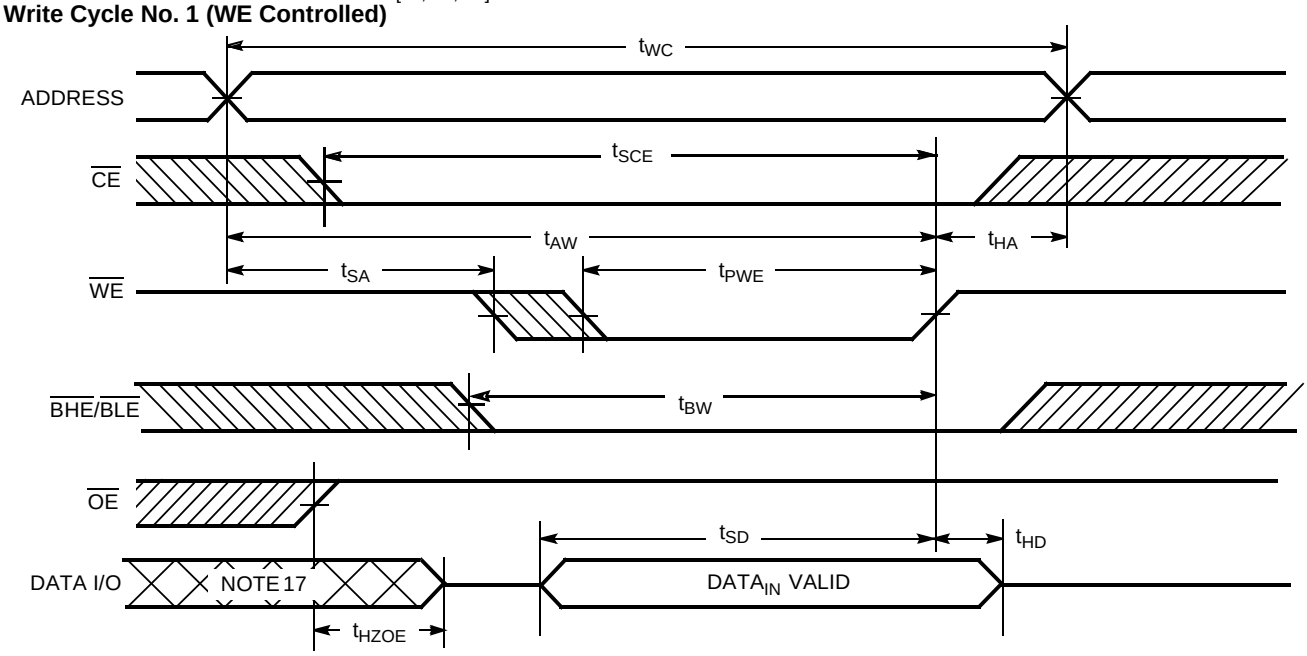
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. It t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
11. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 (OE Controlled) [13, 14]



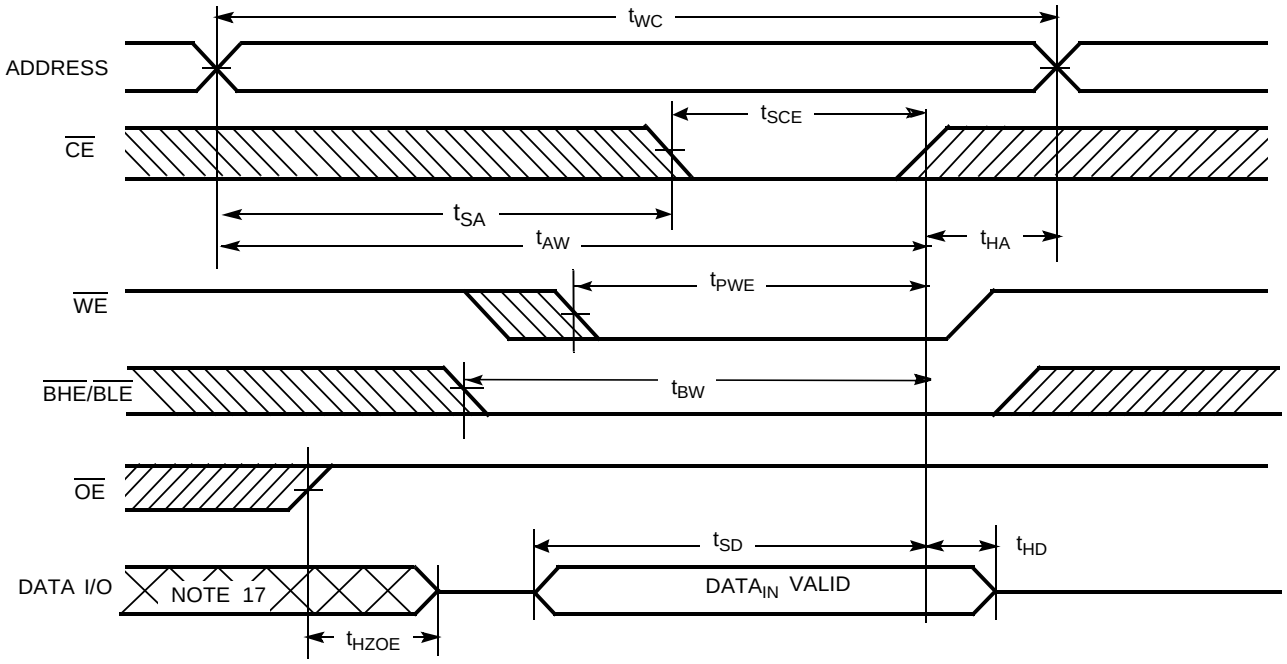
Write Cycle No. 1 (WE Controlled) [11, 15, 16]



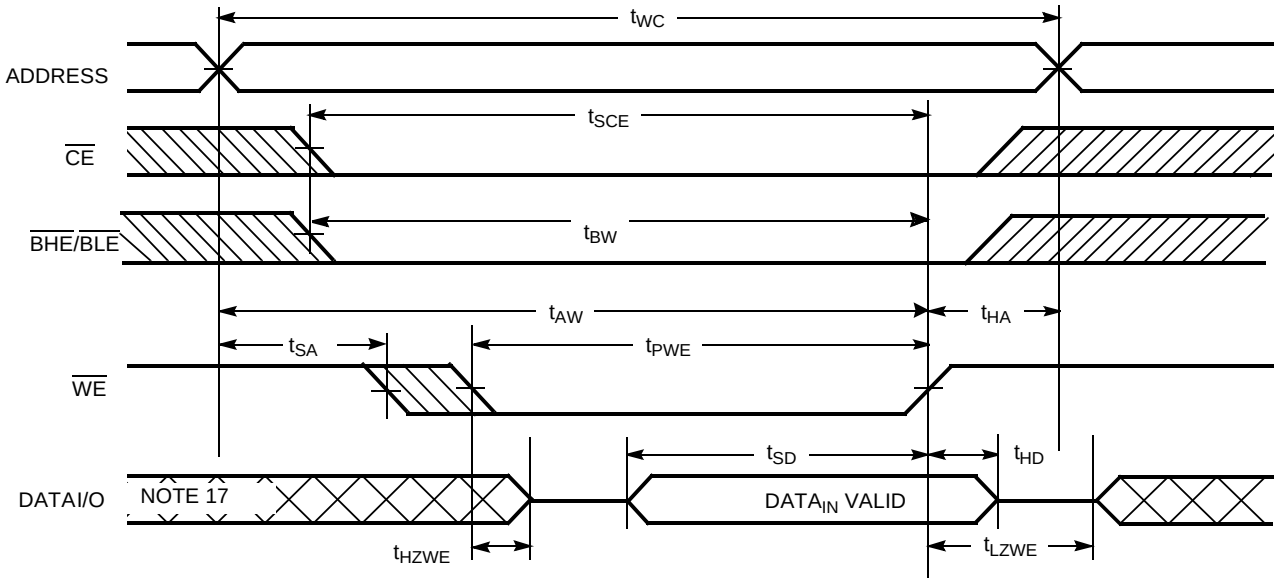
Notes:
14. Address valid prior to or coincident with CE, BHE, BLE transition LOW.
15. Data I/O is high-impedance if OE = V_{IH}.
16. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled) [11, 15, 16]

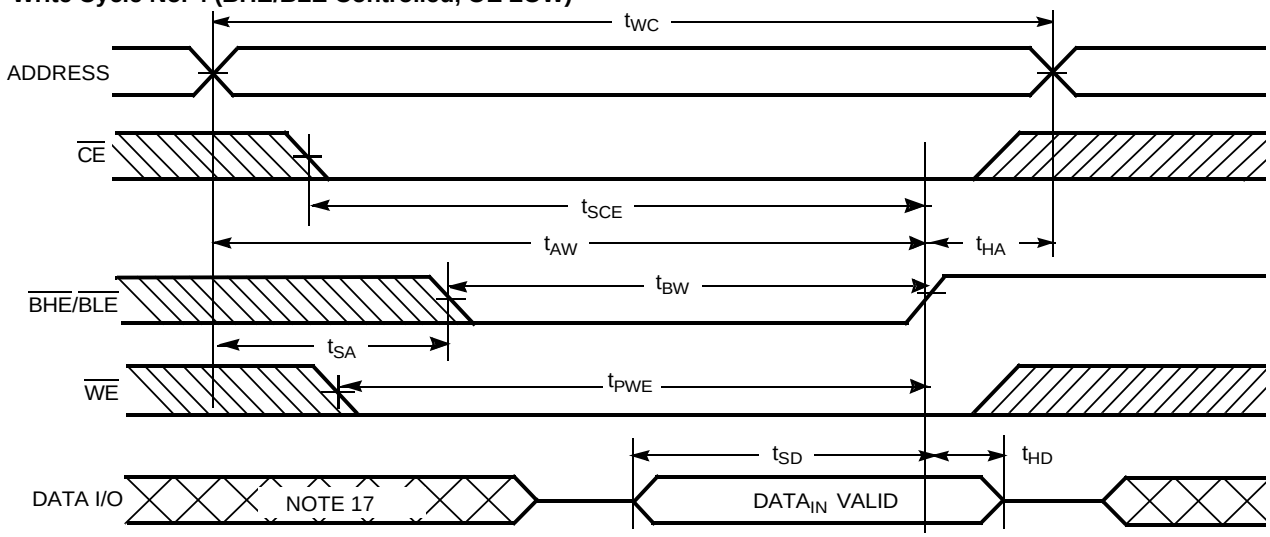


Write Cycle No. 3 (WE Controlled, OE LOW) [16]



Switching Waveforms (continued)

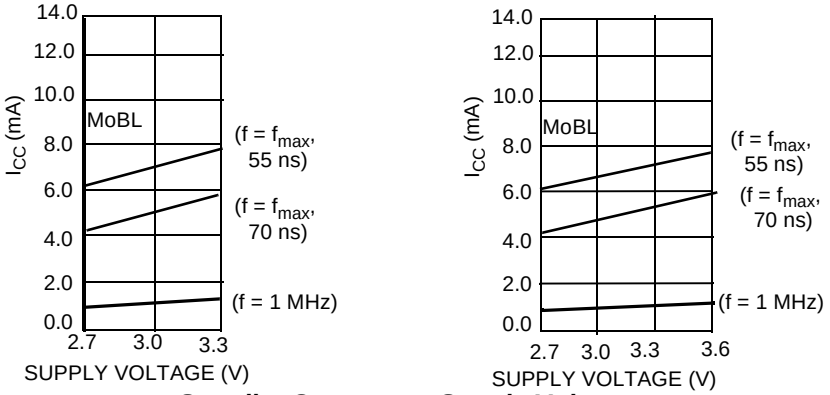
Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[16]



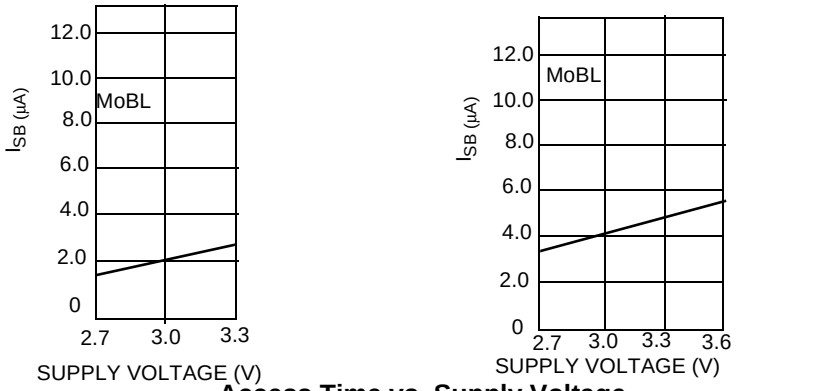
Typical DC and AC Parameters

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$)

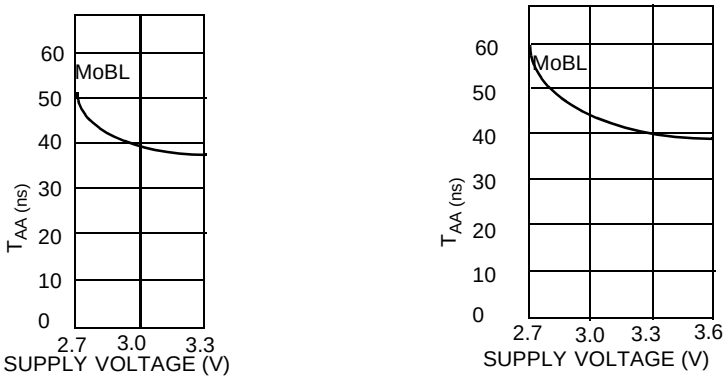
Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output Disabled	Active (I_{CC})

Truth Table (continued)

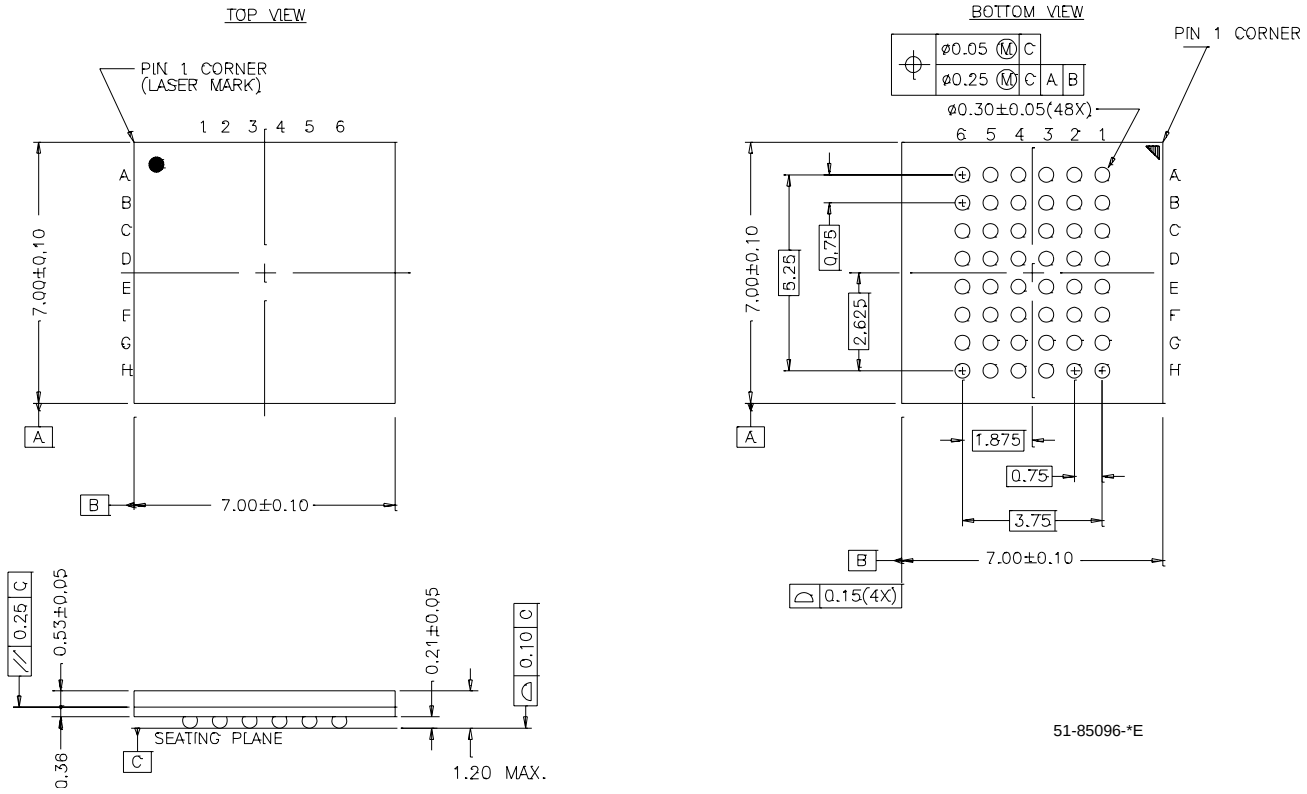
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
L	H	H	H	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Voltage Range (V)	Package Name	Package Type	Operating Range
70	CY62136CV30LL-70BAI	2.7–3.3	BA48A	48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	Industrial
	CY62136CV30LL-70BVI	2.7–3.3	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62136CV33LL-70BAI	3.0–3.6	BA48A	48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62136CV33LL-70BVI	3.0–3.6	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62136CVLL-70BAI	2.7–3.6	BA48A	48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62136CVLL-70BVI	2.7–3.6	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62136CV30LL-55BAI	2.7–3.3	BA48A	48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62136CV30LL-55BVI	2.7–3.3	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62136CV33LL-55BAI	3.0–3.6	BA48A	48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62136CV33LL-55BVI	3.0–3.6	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

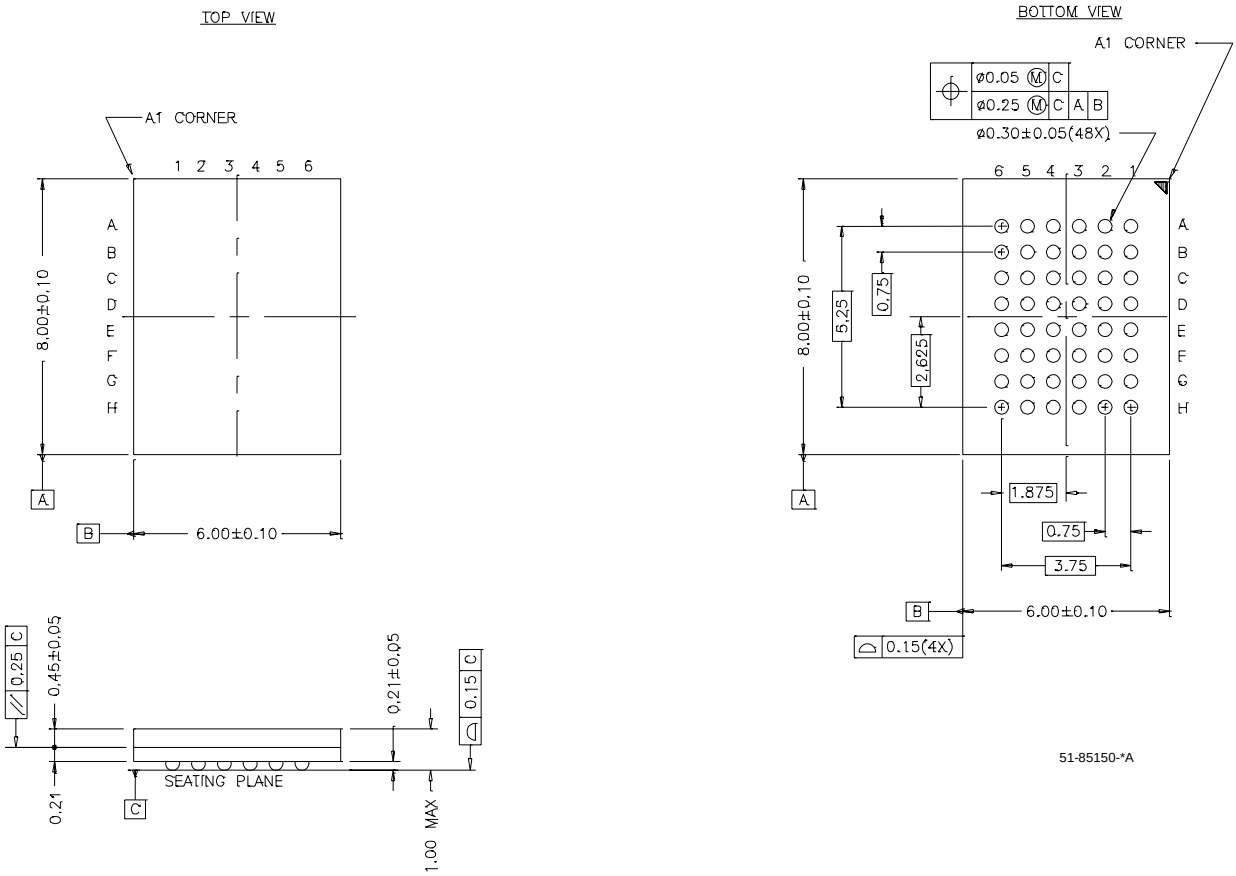
Package Diagrams

48-ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A



Package Diagrams (continued)

48-ball VFBGA (6 x 8 x 1 mm) BV48A



Document History Page

Document Title: CY62136CV30/33/CY62136CV/CY62136CV30/33 2M (128K x 16) Static RAM Document Number: 38-05199				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112379	02/19/02	GAV	New Data Sheet (advance information)
*A	114023	04/25/02	JUI	Added BV package diagram Changed Advance Information to Preliminary
*B	117063	07/12/02	MGN	Changed Preliminary to Final
*C	118121	08/26/02	MGN	Added new part numbers: CY62136CV with wider voltage (2.7V – 3.6V); CY62136CV33 narrower voltage range (3.0V – 3.6V) For T_{AA} = 55 ns, improved t_{PWE} Min from 45 ns to 40 ns For T_{AA} = 70 ns, improved t_{PWE} Min from 50 ns to 45 ns For T_{AA} = 70 ns, improved t_{LZWE} Min from 5 ns to 10 ns
*D	118622	10/3/02	MGN	Improved Typ. I_{CC} spec. to 7 mA (for 55 ns) and 5.5 mA (for 70 ns) Improved Max I_{CC} spec. to 15 mA (for 55 ns) and 12 mA (for 70 ns) For T_{AA} = 55 ns, improved t_{LZWE} min. from 5 ns to 10 ns Changed upper spec. for Supply Voltage to Ground Potential to V_{CCMAX} + 0.5V Changed upper spec. for DC Voltage Applied to Outputs in High-Z State and DC Input Voltage to V_{CC} + 0.3V