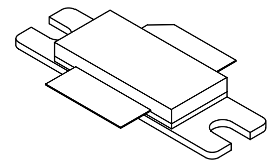
The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

MRF18085BR3
MRF18085BLSR3

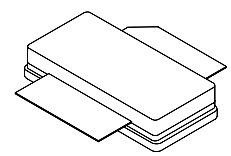
Designed for GSM and GSM EDGE base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA, and multicarrier amplifier applications.

- GSM and GSM EDGE Performance, Full Frequency Band (1930 - 1990 MHz)
  Power Gain - 12.5 dB (Typ) @ 85 Watts CW
  Efficiency - 50% (Typ) @ 85 Watts CW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency, and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, @ P1dB Output Power, @ f = 1930 MHz
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40µ″ Nominal.
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

GSM/GSM EDGE
1.9 - 1.99 GHz, 85 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF18085BR3



CASE 465A-06, STYLE 1
NI-780S
MRF18085BLSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	273 1.56	Watts W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.79	°C/W

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

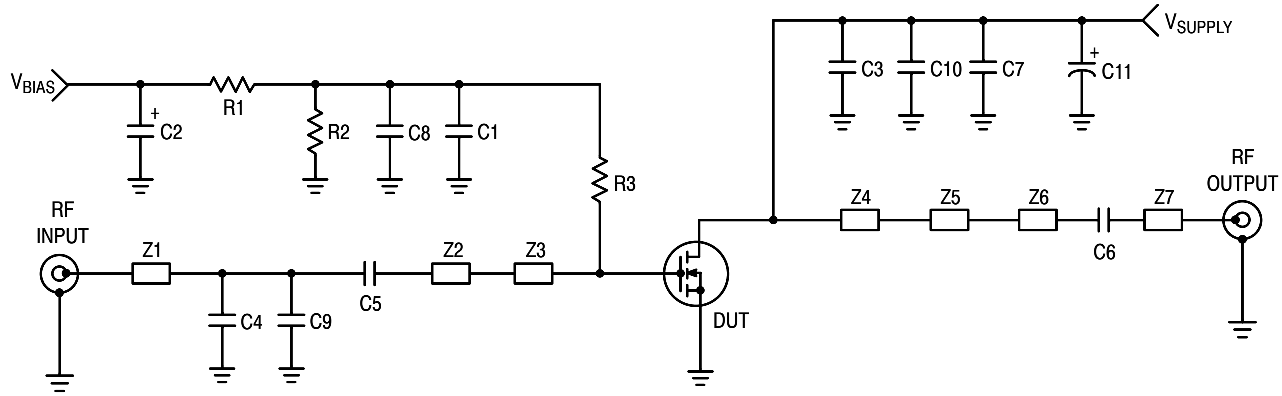
(1) Refer to AN1955/D, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.motorola.com/semiconductors/rf. Select Documentation/Application Notes - AN1955.

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 600 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.18	0.21	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	6.0	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.6	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Common-Source Amplifier Power Gain @ 85 W (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1930 - 1990 MHz)	G_{ps}	11.5	12.5	—	dB
Drain Efficiency @ 85 W (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1930 - 1990 MHz)	η	46	50	—	%
Input Return Loss @ 85 W (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1930 - 1990 MHz)	IRL	—	-12	-9	dB
P1 dB Output Power (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1930 - 1990 MHz)	P1dB	80	90	—	Watts
Output Mismatch Stress @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



C1, C10	1.0 nF Chip Capacitors, B Case, ATC	Z1	1.654″ x 0.082″ Microstrip
C2	10 μF, 35 V Tantalum Capacitor	Z2	0.207″ x 0.082″ Microstrip
C3, C6	10 pF Chip Capacitors, B Case, ATC	Z3	0.362″ x 1.260″ Microstrip
C4	3.3 pF Chip Capacitor, B Case, ATC	Z4	0.583″ x 0.669″ Microstrip
C5	4.7 pF Chip Capacitor, B Case, ATC	Z5	0.449″ x 0.179″ Microstrip
C7, C8	100 nF Chip Capacitors, ACCU-P (1206)	Z6	0.877″ x 0.082″ Microstrip
C9	3.9 pF Chip Capacitor, B Case, ATC	Z7	0.326″ x 0.082″ Microstrip
C11	470 μF, 63 V Electrolytic Capacitor	PCB	0.030″ Glass Teflon® (ε_r = 2.55)
R1, R2	1.0 kΩ Chip Resistors (0805)		
R3	2 x 18 kΩ Chip Resistor (1206)		

Figure 1. 1.93 - 1.99 GHz Test Fixture Schematic

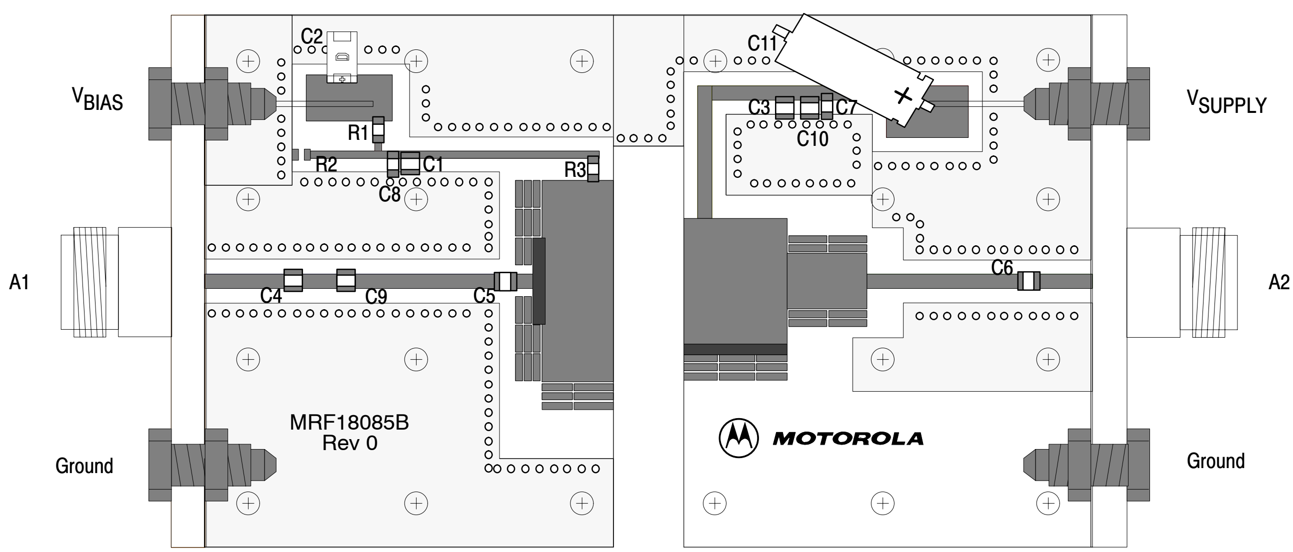
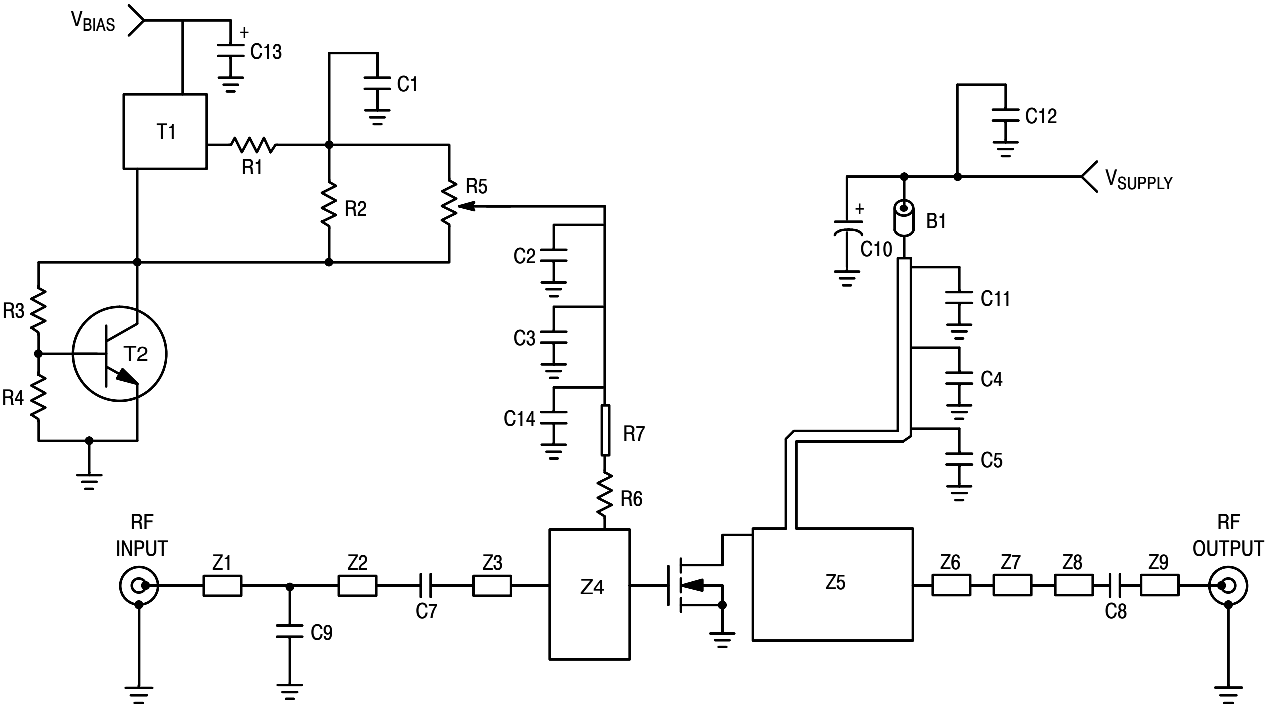


Figure 2. 1.93 - 1.99 GHz Test Fixture Component Layout



B1	Short RF Ferrite Bead, #27 430119447	R1	10 Ω Chip Resistor (0805)
C1, C2	1 μF Chip Capacitors, ACCU-P (0805)	R2	1 kΩ Chip Resistor (0805)
C3, C4	1 nF Chip Capacitors, ACCU-P (0805)	R3	1.2 kΩ Chip Resistor (0805)
C5	10 pF Chip Capacitor, ACCU-P (0805)	R4	2.2 kΩ Chip Resistor (0805)
C7	1.5 pF Chip Capacitor, ACCU-P (0805)	R5	5 kΩ Chip Resistor (0805)
C8	8.2 pF Chip Capacitor, ACCU-P (0805)	R6, R7	9 Ω Chip Resistors (1206) (18 Ω x 18 Ω)
C9	1.0 pF Chip Capacitor, ACCU-P (0805)	T1	Voltage Regulator, Micro-8, Motorola #LP2951
C10	100 μF, 63 V Electrolytic Capacitor	T2	NPN Bipolar Transistor, SOT-23, Motorola #BC847
C11, C12	10 nF Chip Capacitors (0805)	Z1 - Z9	Printed Transmission Lines
C13	10 μF, 35 V Tantalum Capacitor	Substrate	0.5 mm Rogers 4350 (ε_r = 3.53)
C14	8.2 pF Chip Capacitor, ACCU-P (0805)		

Figure 3. 1.93 - 1.99 GHz GSM EDGE Optimized Demo Board Schematic

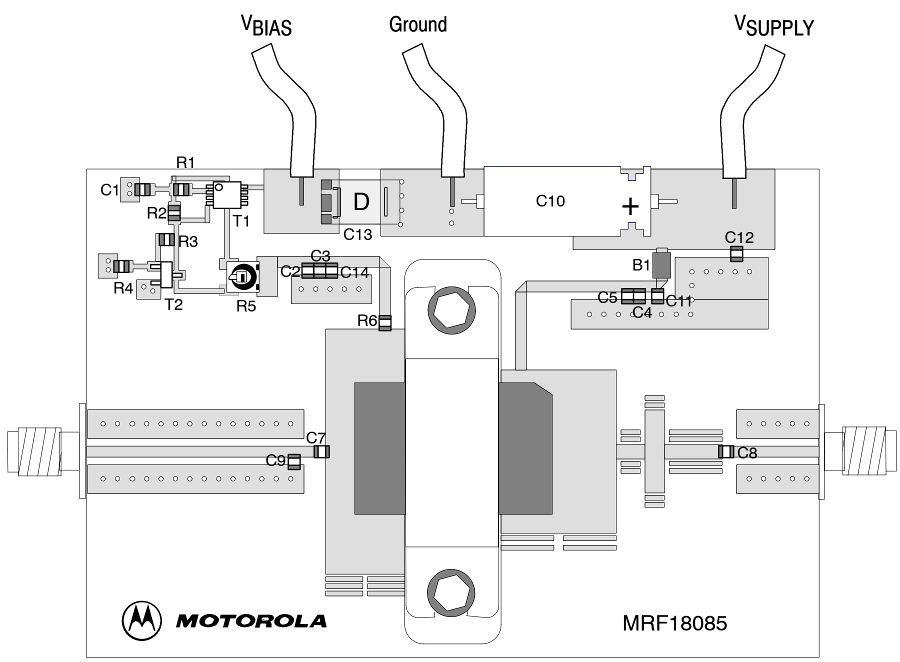


Figure 4. 1.93 - 1.99 GHz GSM EDGE Optimized Demo Board Component Layout

TYPICAL CHARACTERISTICS
(Performed on a GSM EDGE Optimized Demo Board)

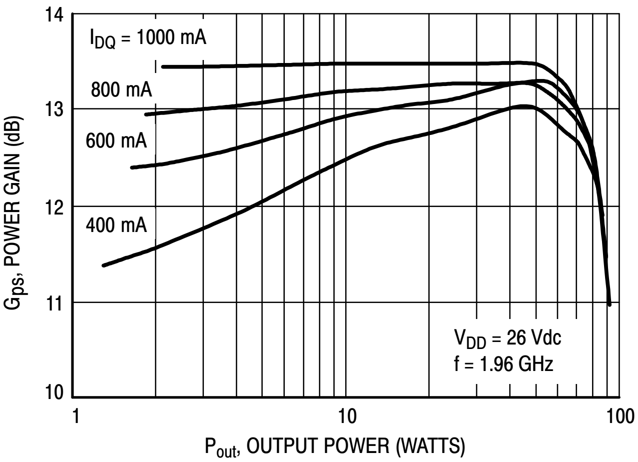


Figure 5. Power Gain versus Output Power

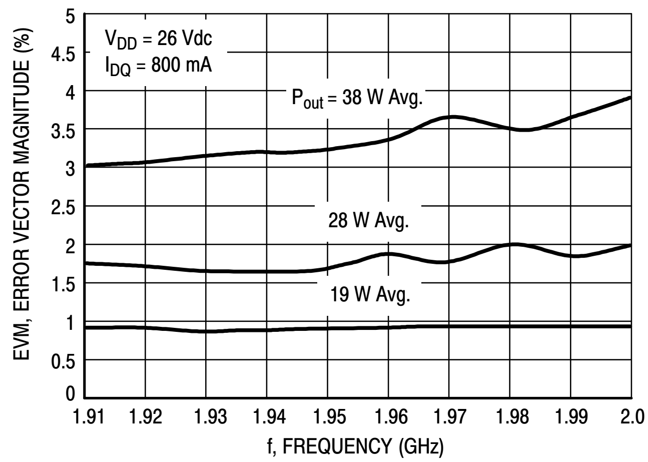


Figure 6. Error Vector Magnitude versus Frequency

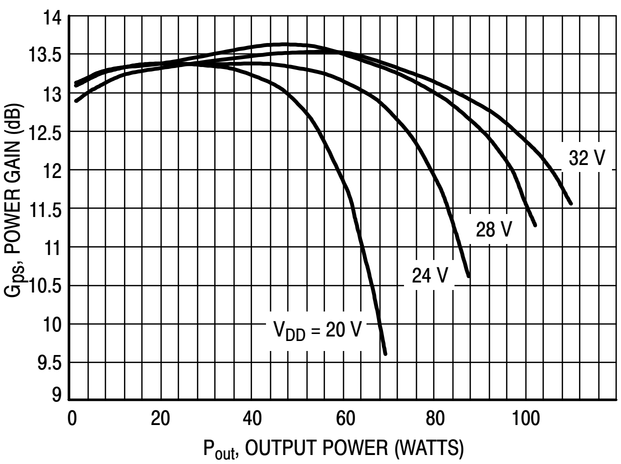


Figure 7. Power Gain versus Output Power

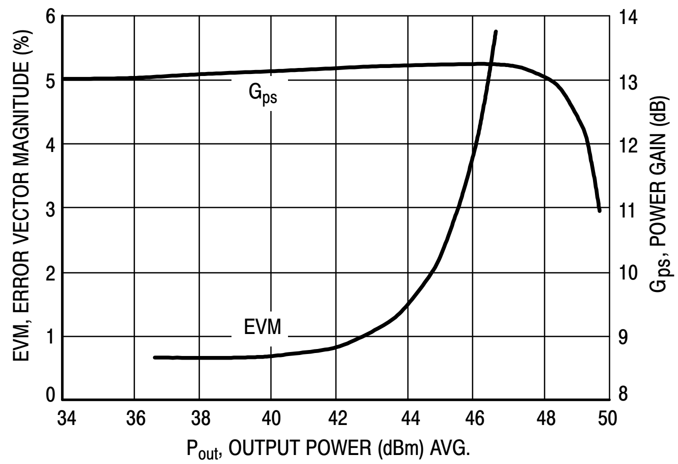


Figure 8. EVM and Gain versus Output Power

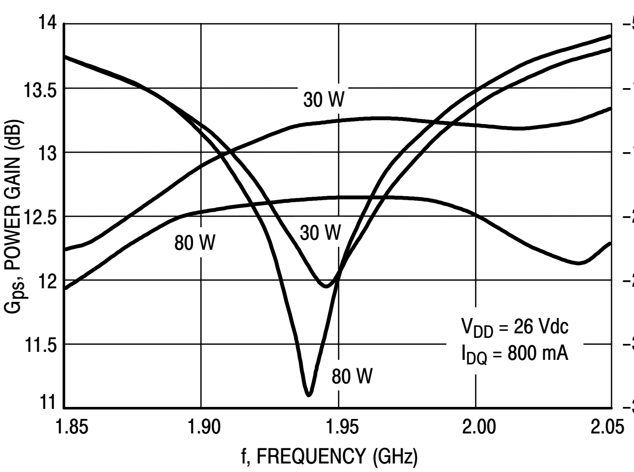


Figure 9. Power Gain and IRL versus Frequency

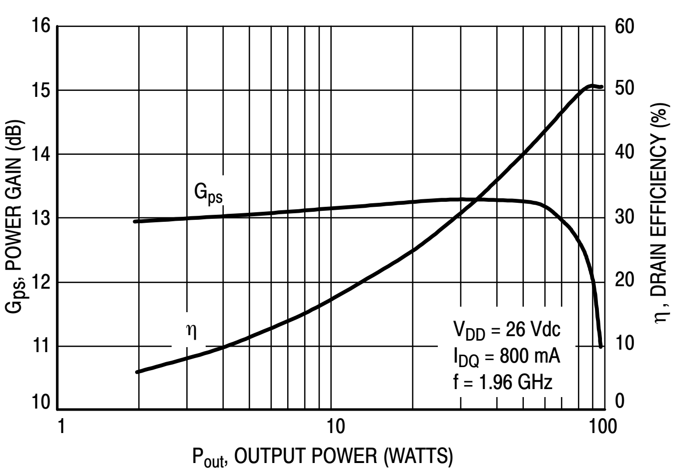


Figure 10. Power Gain and Efficiency versus Output Power

TYPICAL CHARACTERISTICS
(Performed on a GSM EDGE Optimized Demo Board)

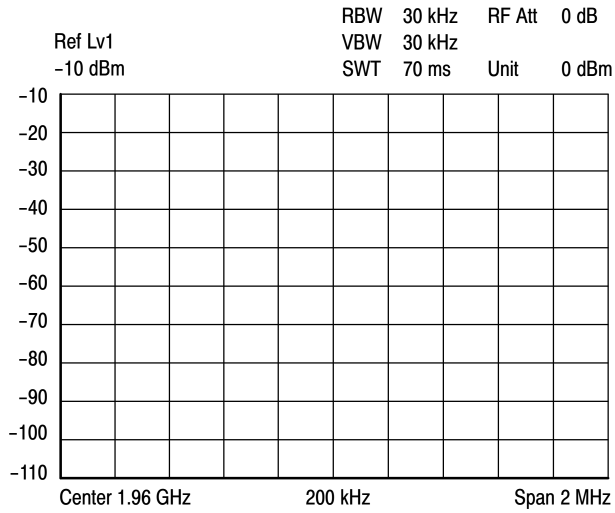
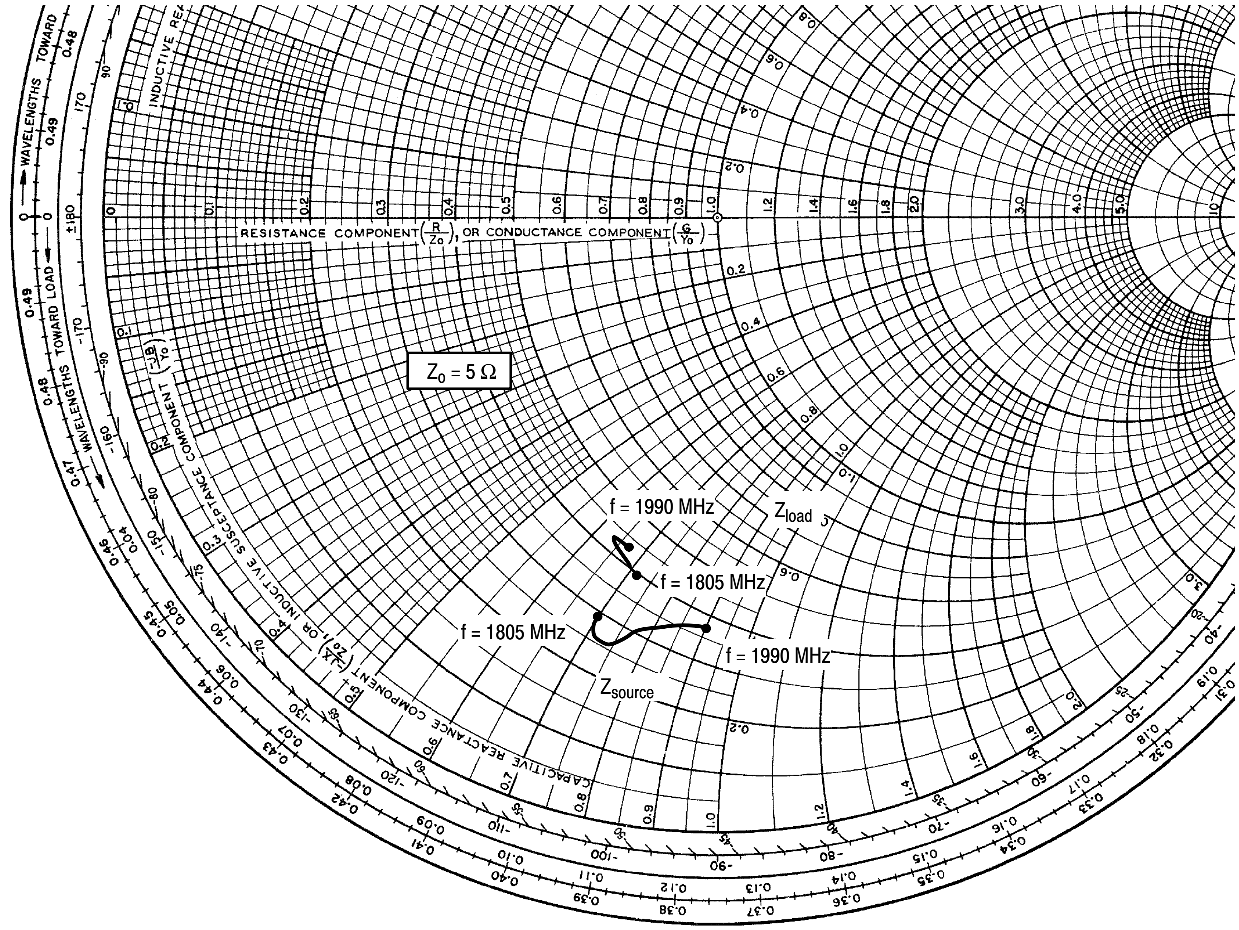


Figure 11. EDGE Spectrum at 40 Watts (Avg.) Output Power



V_{DD} = 26 V, I_{DQ} = 800 mA, P_{out} = 85 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
1805	1.43 - j3.74	2 - j3.60
1880	1.27 - j3.95	1.98 - j3.57
1930	1.5 - j4.13	2.13 - j3.16
1990	1.86 - j4.76	2.17 - j3.36

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

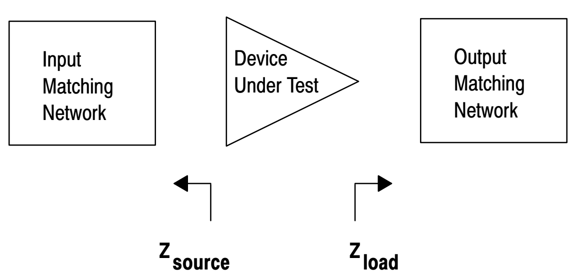


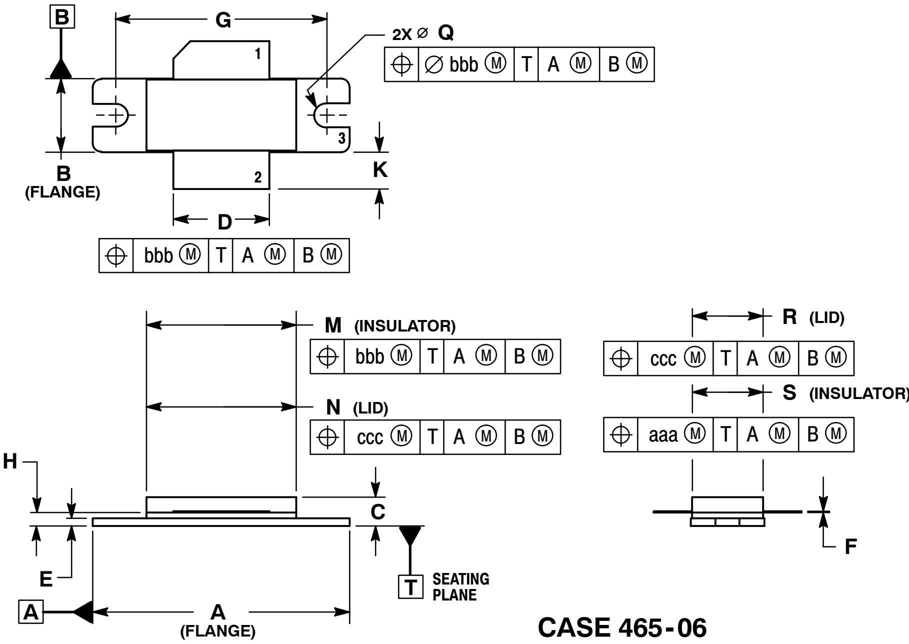
Figure 12. Series Equivalent Input and Output Impedance

NOTES

NOTES

NOTES

PACKAGE DIMENSIONS

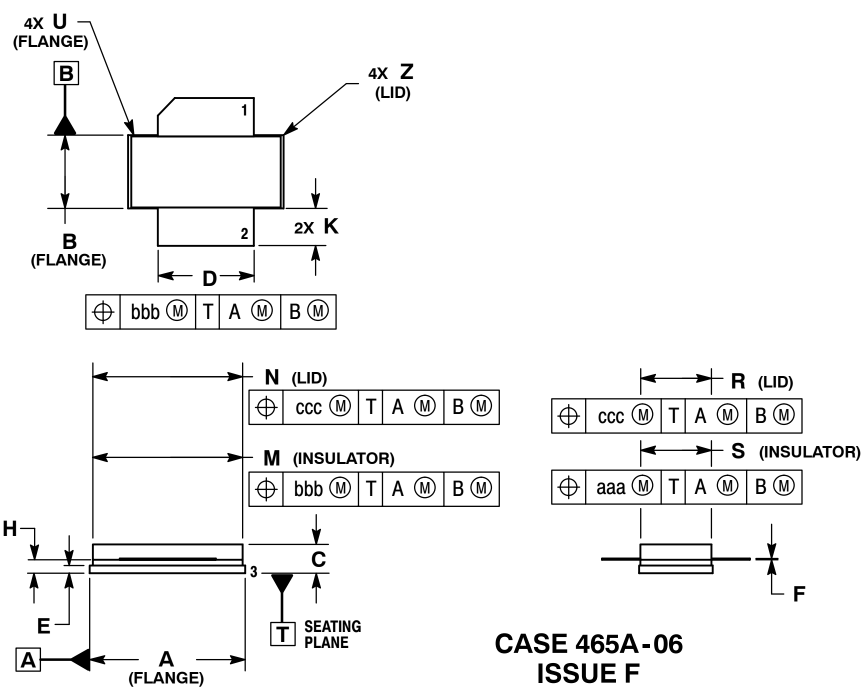


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465-06
ISSUE F
NI-780
MRF18085BR3



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2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

CASE 465A-06
ISSUE F
NI-780S
MRF18085BLSR3

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