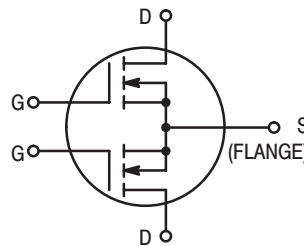


The RF MOSFET Line
RF Power
Field-Effect Transistor
N-Channel Enhancement-Mode MOSFET

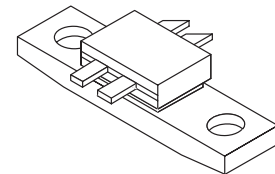
Designed for wideband large-signal amplifier and oscillator applications up to 400 MHz range, in either single ended or push-pull configuration.

- Guaranteed 28 Volt, 150 MHz Performance
Output Power = 30 Watts
Broadband Gain = 14 dB (Typ)
Efficiency = 54% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Space Saving Package For Push-Pull Circuit Applications
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques



MRF136Y

30 W, to 400 MHz
N-CHANNEL
MOS BROADBAND
RF POWER FET



CASE 319B-02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 M\Omega$)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	± 40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	100 0.571	Watts W/ $^\circ C$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ C$
Operating Junction Temperature	T_J	200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^\circ C/W$

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Drain–Source Breakdown Voltage ($V_{GS} = 0, I_D = 5.0 \text{ mA}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero–Gate Voltage Drain Current ($V_{DS} = 28 \text{ V}, V_{GS} = 0$)	I_{DSS}	—	—	2.0	mAdc
Gate–Source Leakage Current ($V_{GS} = 40 \text{ V}, V_{DS} = 0$)	I_{GSS}	—	—	1.0	μAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage ($V_{DS} = 10 \text{ V}, I_D = 25 \text{ mA}$)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ V}, I_D = 250 \text{ mA}$)	g_{fs}	250	400	—	mmhos

DYNAMIC CHARACTERISTICS (1)

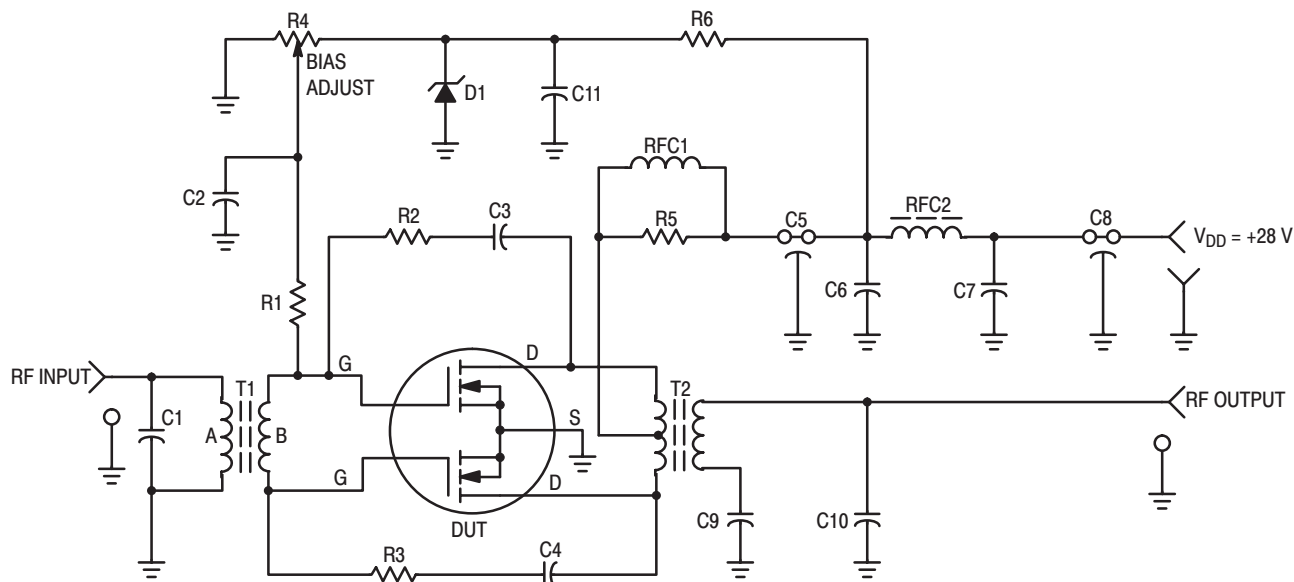
Input Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{iss}	—	24	—	pF
Output Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{rss}	—	5.5	—	pF

FUNCTIONAL CHARACTERISTICS (2)

Common Source Power Gain (Figure 1) ($V_{DD} = 28 \text{ Vdc}, P_{out} = 30 \text{ W}, f = 150 \text{ MHz}, I_{DQ} = 100 \text{ mA}$)	G_{ps}	12	14	—	dB
Drain Efficiency (Figure 1) ($V_{DD} = 28 \text{ Vdc}, P_{out} = 30 \text{ W}, f = 150 \text{ MHz}, I_{DQ} = 100 \text{ mA}$)	η	50	54	—	%
Electrical Ruggedness (Figure 1) ($V_{DD} = 28 \text{ Vdc}, P_{out} = 30 \text{ W}, f = 150 \text{ MHz}, I_{DQ} = 100 \text{ mA},$ VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:

- Each side measured separately.
- Measured in push–pull configuration.



- C1 — 5.0 pF
- C2, C3, C4, C6, C7, C9, C11 — 0.1 μ F Ceramic
- C5, C8 — 680 pF Feedthru
- C10 — 15 pF
- D1 — 1N4740 Motorola Zener
- RFC1 — 17 Turns, #24 AWG Wound on R5
- RFC2 — Ferroxcube VK-200-19/4B or Equivalent
- R1 — 10 k Ω , 1/4 W
- R2, R3 — 560 Ω , 1/2 W
- R4 — 10 Turns, 10 k Ω

- R5 — 56 k Ω , 1 W
- R6 — 1.6 k Ω , 1/4 W
- T1 — Primary Winding — 3 Turns #28 Enameled Wire.
— Secondary Winding — 2 Turns #28 Enameled Wire.
Both windings wound through a Fair/Rite Balun 65 core.
Part #2865002402.
- T2 — 1:1 Transformer Wound Bifilar — 2 Turns Twisted Pair
#24 Enameled Wire through a Indiana General Balun Q1
core. Part #18006-1-Q1. Primary winding center tapped.
- Board Material — 0.062" G10, 1 oz. Cu Clad, Double Sided

Figure 1. 30-150 MHz Test Circuit

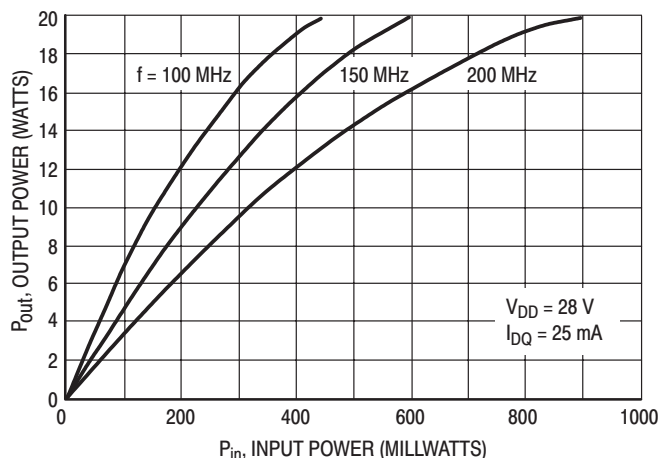


Figure 2. Output Power versus Input Power

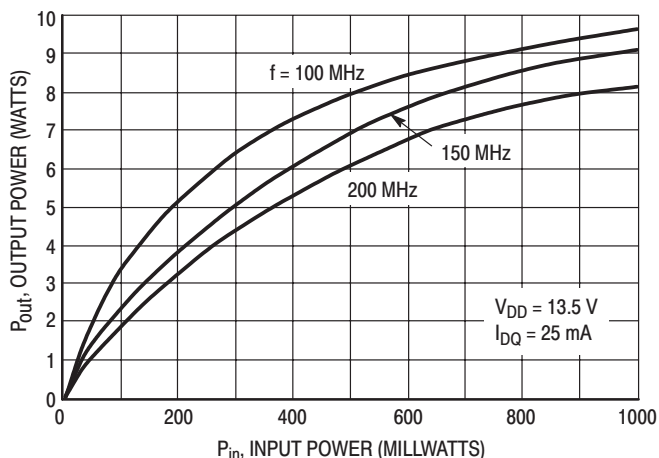


Figure 3. Output Power versus Input Power

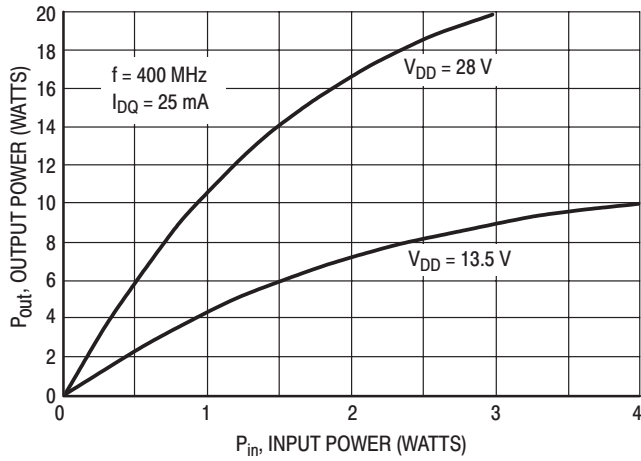


Figure 4. Output Power versus Input Power

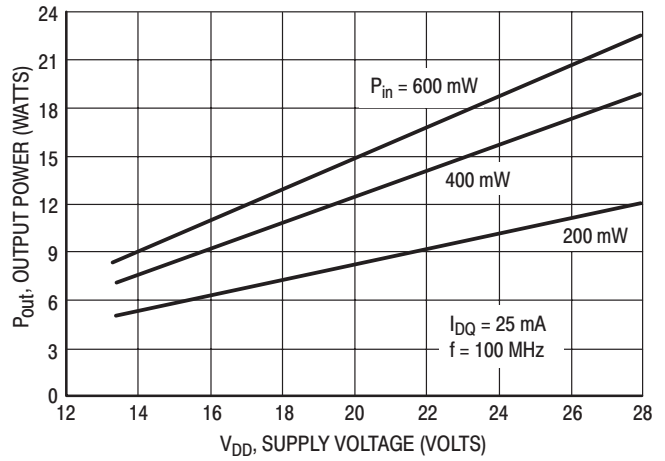


Figure 5. Output Power versus Supply Voltage

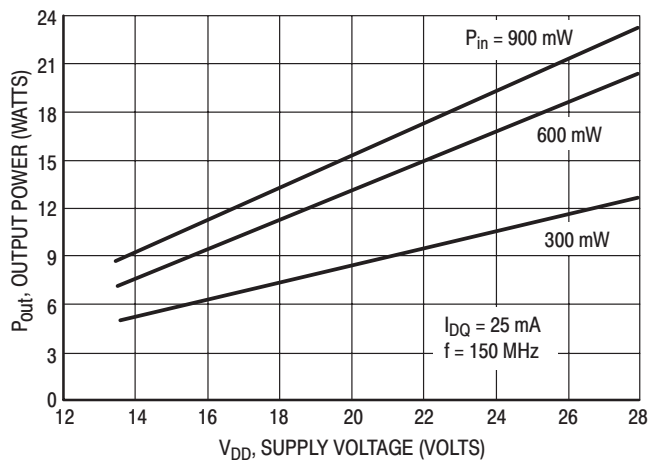


Figure 6. Output Power versus Supply Voltage

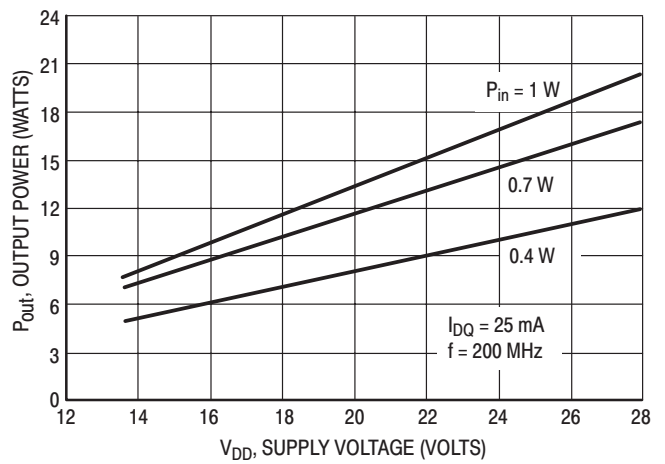


Figure 7. Output Power versus Supply Voltage

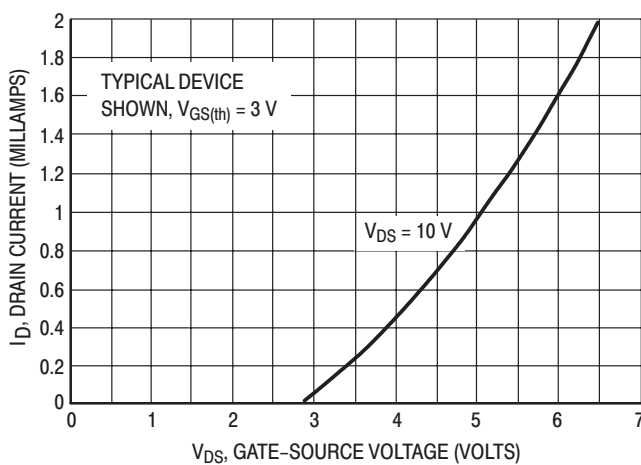


Figure 8. Drain Current versus Gate Voltage (Transfer Characteristics)*

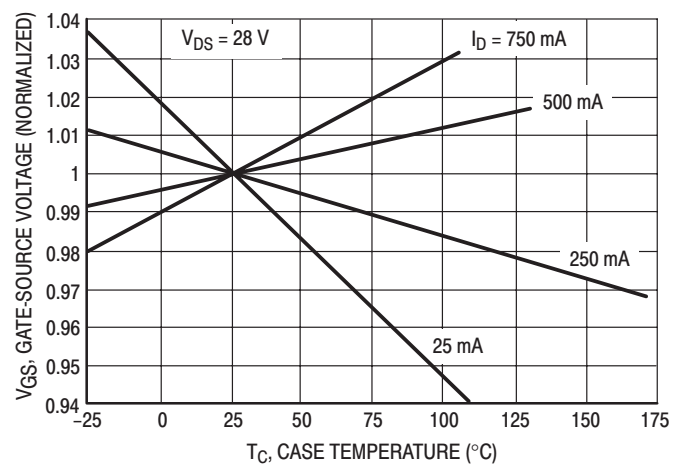


Figure 9. Gate-Source Voltage versus Case Temperature*

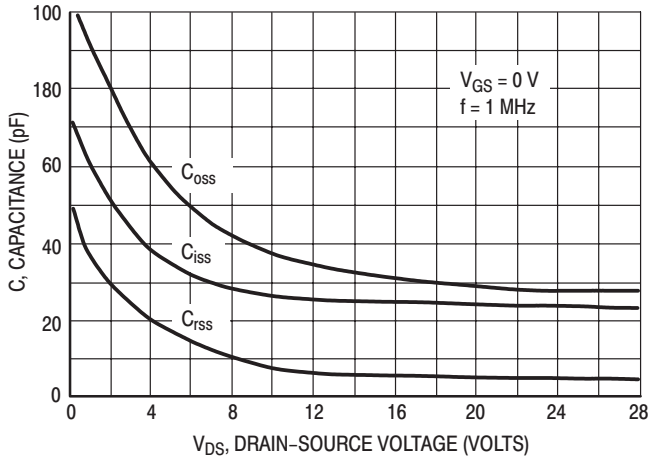


Figure 10. Capacitance versus Drain-Source Voltage

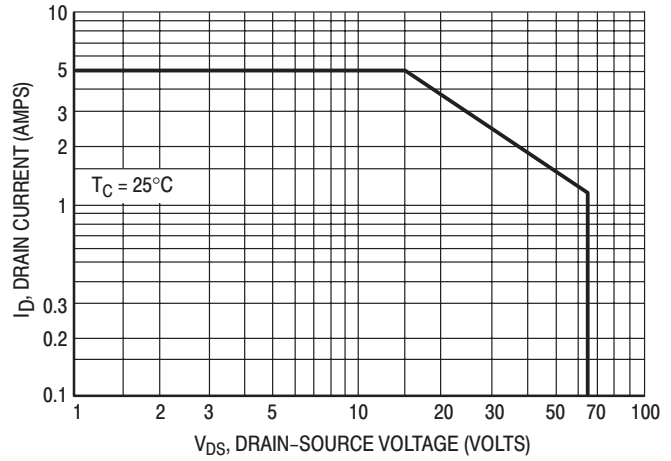


Figure 11. DC Safe Operating Area

**TYPICAL PERFORMANCE IN BROADBAND TEST CIRCUIT
(Refer to Figure 1)**

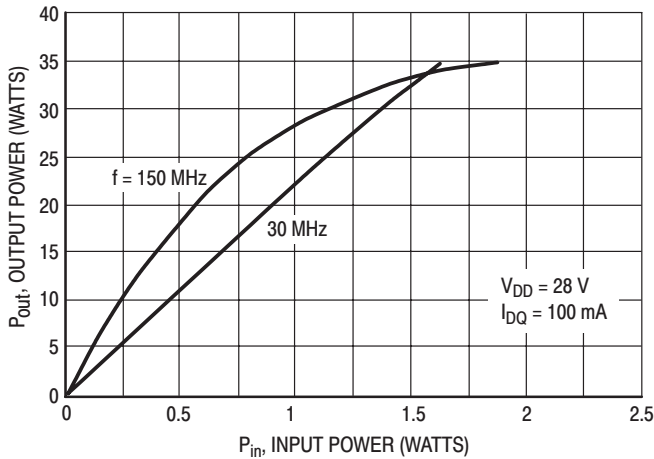


Figure 12. Output Power versus Input Power

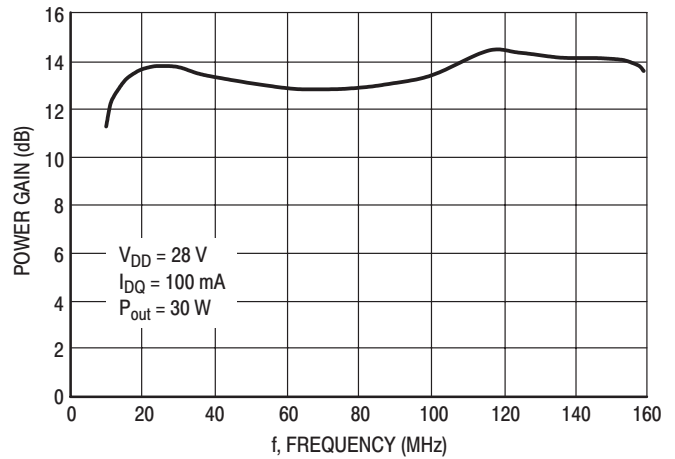


Figure 13. Power Gain versus Frequency

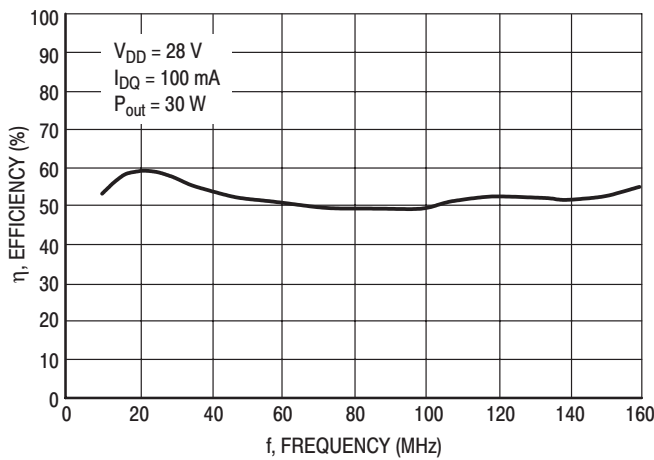


Figure 14. Drain Efficiency versus Frequency

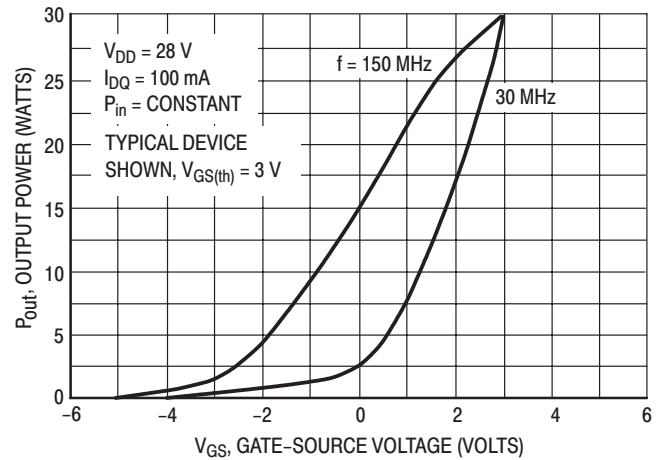


Figure 15. Output Power versus Gate Voltage

TYPICAL 400 MHz PERFORMANCE

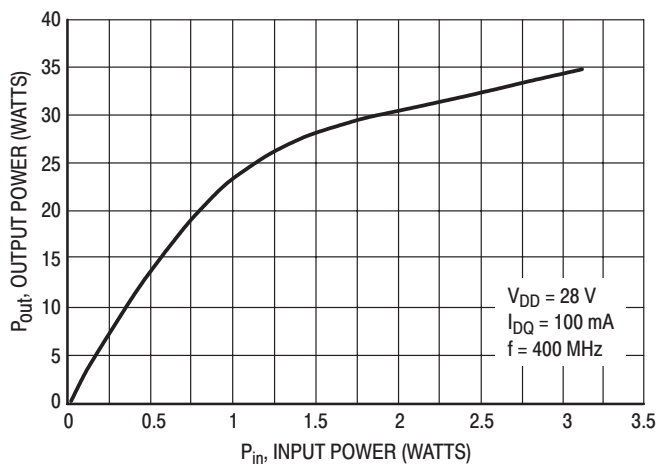


Figure 16. Output Power versus Input Power

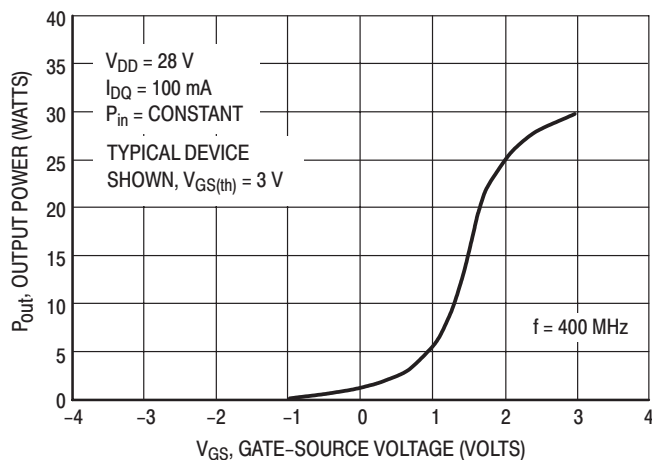


Figure 17. Output Power versus Gate Voltage

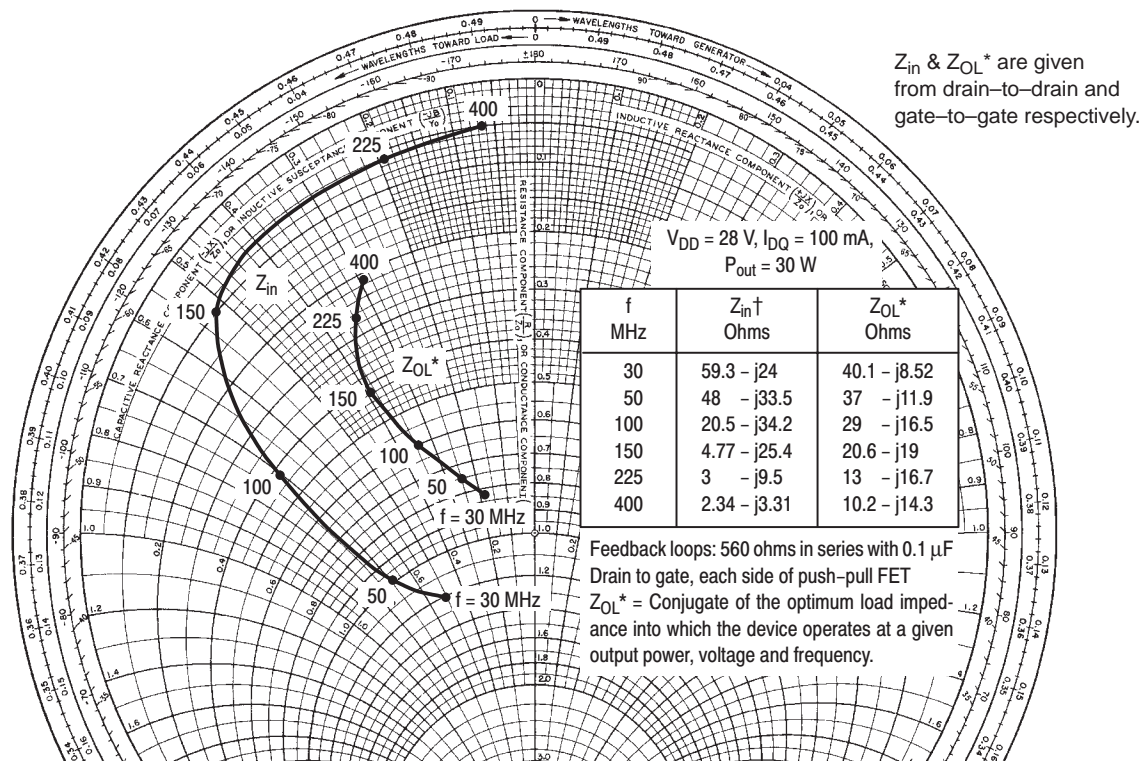


Figure 18. Input and Output Impedance

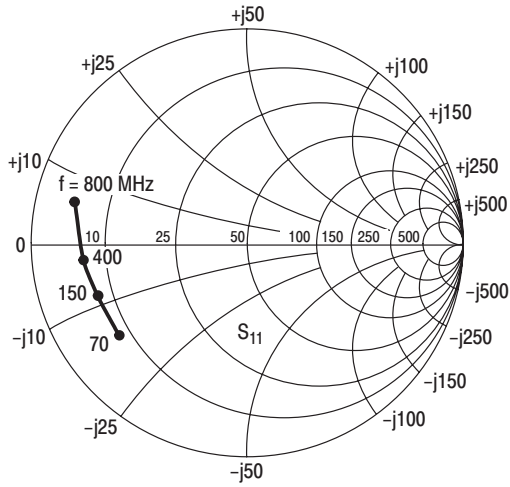


Figure 19. S_{11} , Input Reflection Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

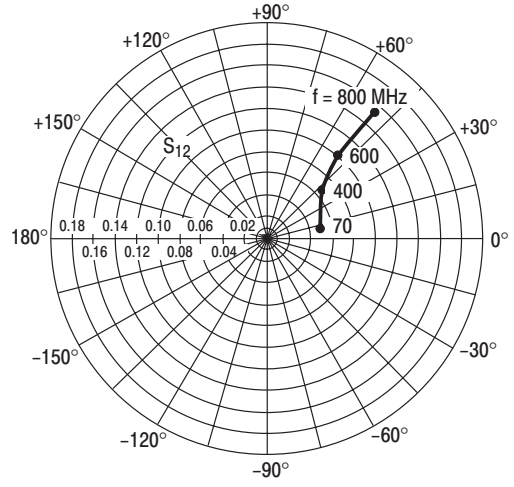


Figure 20. S_{12} , Reverse Transmission Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

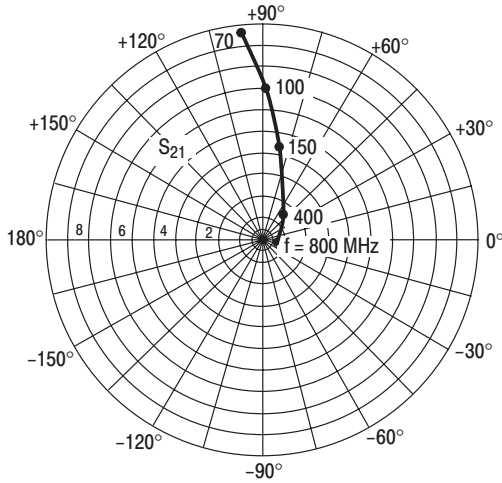


Figure 21. S_{21} , Forward Transmission Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

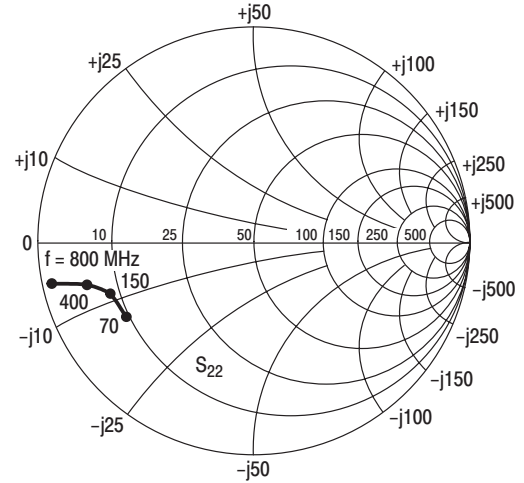


Figure 22. S_{22} , Output Reflection Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

DESIGN CONSIDERATIONS

The MRF136Y is an RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for HF and VHF power amplifier applications. M/A-COM RF MOS FETs feature planar design for optimum manufacturability.

M/A-COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF136Y is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied without gate bias. A positive gate voltage causes drain current to flow (see Figure 8). RF power FETs require forward bias for optimum gain and power output. A Class AB condition with quiescent drain current (I_{DQ}) in the 25–100 mA range is sufficient for many applications. For special requirements such as linear amplification, I_{DQ} may have to be adjusted to optimize the critical parameters.

The MOS gate is a dc open circuit. Since the gate bias circuit does not have to deliver any current to the FET, a simple resistive divider arrangement may sometimes suffice for this function. Special applications may require more elaborate gate bias systems.

GAIN CONTROL

Power output of the MRF136Y may be controlled from rated values down to the milliwatt region (>20 dB reduction in power output with constant input power) by varying the dc gate

voltage. This feature, not available in bipolar RF power devices, facilitates the incorporation of manual gain control, AGC/ALC and modulation schemes into system designs. A full range of power output control may require dc gate voltage excursions into the negative region.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF136Y. See M/A-COM Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. Large signal impedance parameters are provided. Large signal impedances should be used for network designs wherever possible. While the s parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is particularly useful at frequencies outside those presented in the large signal impedance plots.

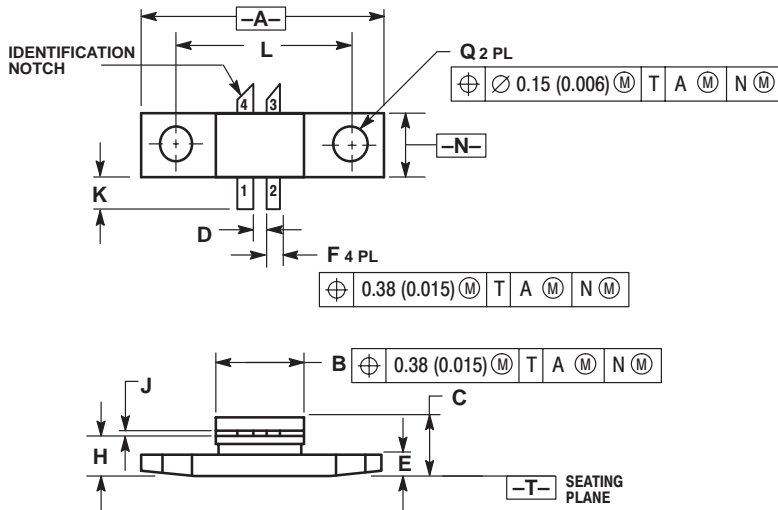
RF power FETs are triode devices and are therefore not unilateral. This, coupled with the very high gain, yields a device capable of self oscillation. Stability may be achieved using techniques such as drain loading, input shunt resistive loading, or feedback. S parameter stability analysis can provide useful information in the selection of loading and/or feedback to insure stable operation. The MRF136Y was characterized with a resistive feedback loop around each of its two active devices.

For further discussion of RF amplifier stability and the use of two port parameters in RF amplifier design, see M/A-COM Application Note AN215A.

LOW NOISE OPERATION

Input resistive loading will degrade noise performance, and noise figure may vary significantly with gate driving impedance. A low loss input matching network with its gate impedance optimized for lowest noise is recommended.

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.965	0.985	24.51	25.02
B	0.355	0.375	9.02	9.52
C	0.230	0.260	5.84	6.60
D	0.055	0.065	1.40	1.65
E	0.102	0.114	2.59	2.90
F	0.055	0.065	1.40	1.65
H	0.160	0.170	4.06	4.31
J	0.004	0.006	0.10	0.15
K	0.120	0.140	3.05	3.55
L	0.725 BSC		18.42 BSC	
N	0.225	0.241	5.72	6.12
Q	0.125	0.135	3.18	3.42

- STYLE 1:
 PIN 1. GATE (INPUT)
 PIN 2. GATE (INPUT)
 PIN 3. DRAIN (OUTPUT)
 PIN 4. DRAIN (OUTPUT)
 SOURCE IS FLANGE

**CASE 319B-02
 ISSUE C**

Specifications subject to change without notice.

- North America: Tel. (800) 366-2266, Fax (800) 618-8883
- Asia/Pacific: Tel.+81-44-844-8296, Fax +81-44-844-8298
- Europe: Tel. +44 (1344) 869 595, Fax+44 (1344) 300 020

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