

Advance Information

1M x 8 Bit

Fast Static RAM Module

The MCM8A10 is an 8M bit static random access memory module organized as 1,048,576 words of 8 bits. The module is offered in a 72-lead single in-line memory module (SIMM). Eight MCM6227B fast static RAMs, packaged in 28-lead SOJ packages are mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6227B is organized as 1,048,576 words of 1 bit. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM8A10 is equipped with a chip enable (E) and eight separate write enable (W0 – W7) inputs, allowing for greater system flexibility.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 15 ns
- Three-State Outputs
- Fully TTL Compatible
- High Board Density SIMM Package
- Bit Operation: Eight Separate Write Enables, One for Each Bit
- High Quality Six-Layer FR4 PWB with Separate Internal Power and Ground Planes

PIN NAMES	
A0 – A19	Address Inputs
W0 – W7	Write Enables
E	Chip Enable
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
PD0 – PD2	Package Density
DAISY	Pins Single Net
VCC	+ 5 V Power Supply
VSS	Ground

For proper operation of the device, VSS must be connected to ground.

MCM8A10

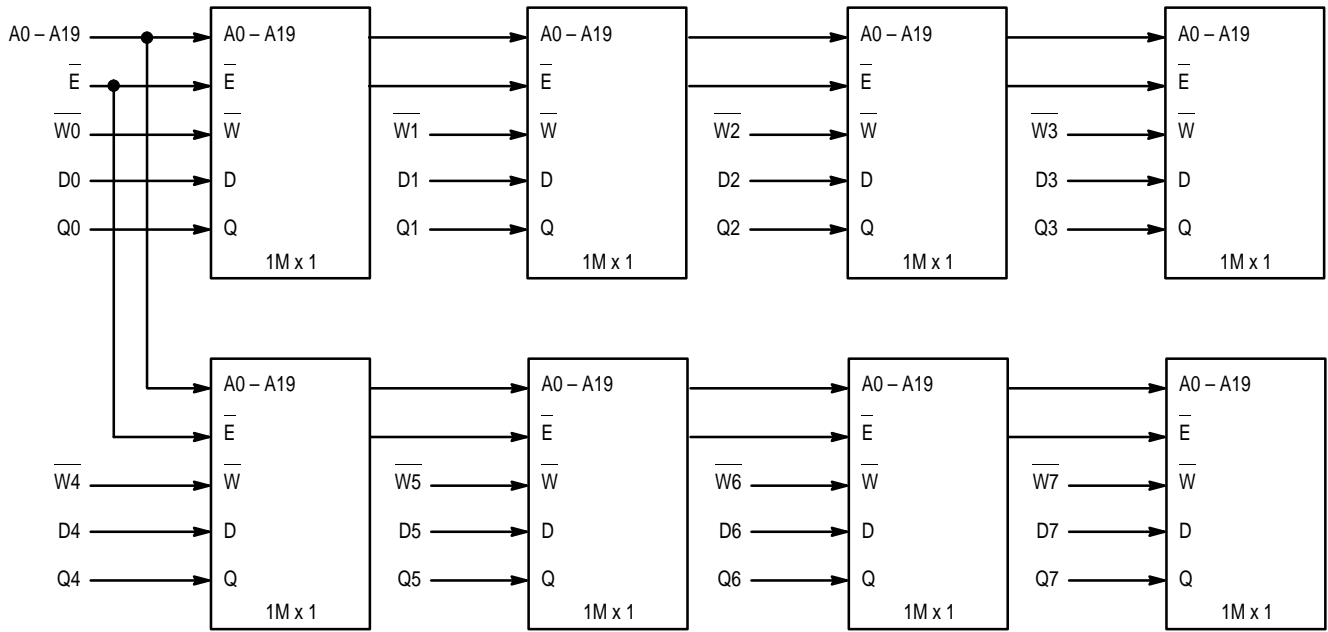
PIN ASSIGNMENT TOP VIEW 72-LEAD SIMM – CASE TBD

A1	2	1	A0
VSS	4	3	A2
A3	6	5	VCC
A5	8	7	A4
A7	10	9	A6
VCC	12	11	VSS
A9	14	13	A8
D0	16	15	Q0
VSS	18	17	W0
W1	20	19	VCC
Q1	22	21	D1
A11	24	23	A10
VCC	26	25	VSS
DAISY	28	27	DAISY
D2	30	29	Q2
VSS	32	31	W2
W3	34	33	VCC
Q3	36	35	D3
PD1	38	37	PD0
VCC	40	39	VSS
Q4	42	41	PD2
W4	44	43	D4
VCC	46	45	VSS
D5	48	47	W5
A21	50	49	Q5
A19	52	51	A20
VCC	54	53	VSS
A17	56	55	A18
A15	58	57	A16
VSS	60	59	A14
A13	62	61	VCC
Q6	64	63	A12
W6	66	65	D6
VCC	68	67	VSS
D7	70	69	W7
E	72	71	Q7

This document contains information on a new product. Specifications and information herein are subject to change without notice.

10/30/96

**FUNCTIONAL BLOCK DIAGRAM
1M x 8 MEMORY MODULE**



PD0 — Open
 PD1 — V_{SS}
 PD2 — Open

TRUTH TABLE

E	W	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High-Z	—	I _{SB1} , I _{SB2}
L	H	Read	D _{out}	Read	I _{CCA}
L	L	Write	High-Z	Write	I _{CCA}

NOTE: H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V _{SS}	V _{CC}	- 0.5 to 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	- 0.5 to V _{CC} + 0.5	V
Output Current	I _{out}	± 20	mA
Power Dissipation	P _D	8.8	W
Temperature Under Bias	T _{bias}	- 10 to + 85	°C
Operating Temperature	T _A	0 to + 70	°C
Storage Temperature	T _{stg}	- 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{CC}	4.75	5.25	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3**	V
Input Low Voltage	V _{IL}	- 0.5*	0.8	V

* V_{IL} (min) = - 0.5 V dc; V_{IL} (min) = - 2.0 V ac (pulse width ≤ 20 ns).

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{CC})	I _{lkg(I)}	—	± 1	μA
Output Leakage Current (E = V _{IH} , V _{out} = 0 to V _{CC})	I _{lkg(O)}	—	± 1	μA
AC Active Supply Current (I _{out} = 0 mA, V _{CC} = max)	I _{CCA}	—	920	mA
AC Standby Current (V _{CC} = max, E = V _{IH} , f ≤ f _{max})	I _{SB1}	—	320	mA
CMOS Standby Current (E ≥ V _{CC} - 0.2 V, V _{in} ≤ V _{SS} + 0.2 V or ≥ V _{CC} - 0.2 V, V _{CC} = max, f = 0 MHz)	I _{SB2}	—	40	mA
Output Low Voltage (I _{OL} = + 8.0 mA)	V _{OL}	—	0.4	V
Output High Voltage (I _{OH} = - 4.0 mA)	V _{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit	
Input Capacitance	Address Inputs E W	C _{in}	42	58	pF
			50	74	
			10	13	
Input and Output Capacitance	D, Q	C _{in} , C _{out}	10	13	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 5\%$, $T_A = 0\text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

Input Pulse Levels 0 to 3.0 V	Output Timing Measurement Reference Level 1.5 V
Input Rise/Fall Time 2 ns	Output Load See Figure 1a
Input Timing Measurement Reference Level 1.5 V	

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM8A10-15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	ns	
Enable Access Time	t_{ELQV}	—	15	ns	4
Output Hold from Address Change	t_{AXQX}	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	0	6	ns	5, 6, 7

NOTES:

1. W is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with E going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured $\pm 500\text{ mV}$ from steady-state voltage with load of Figure 1b.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($E \leq V_{IL}$).

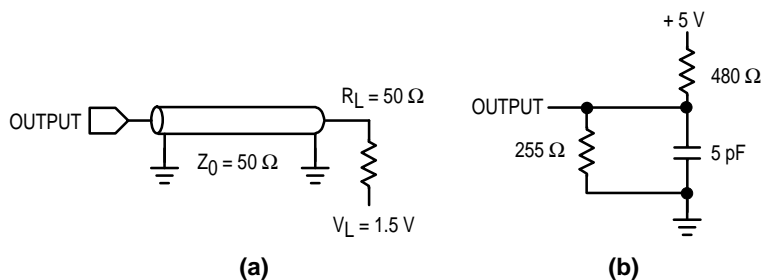
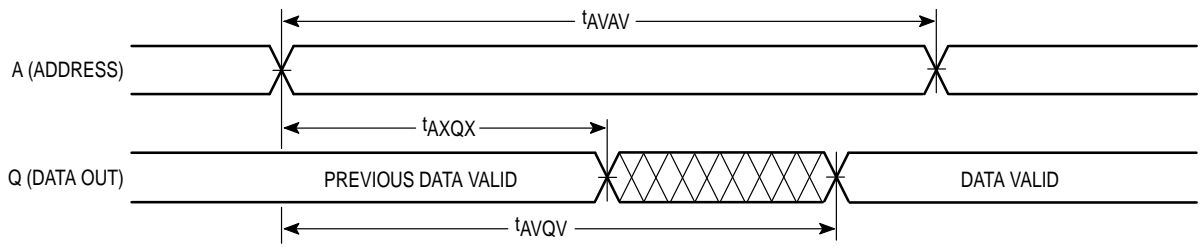


Figure 1. AC Test Loads

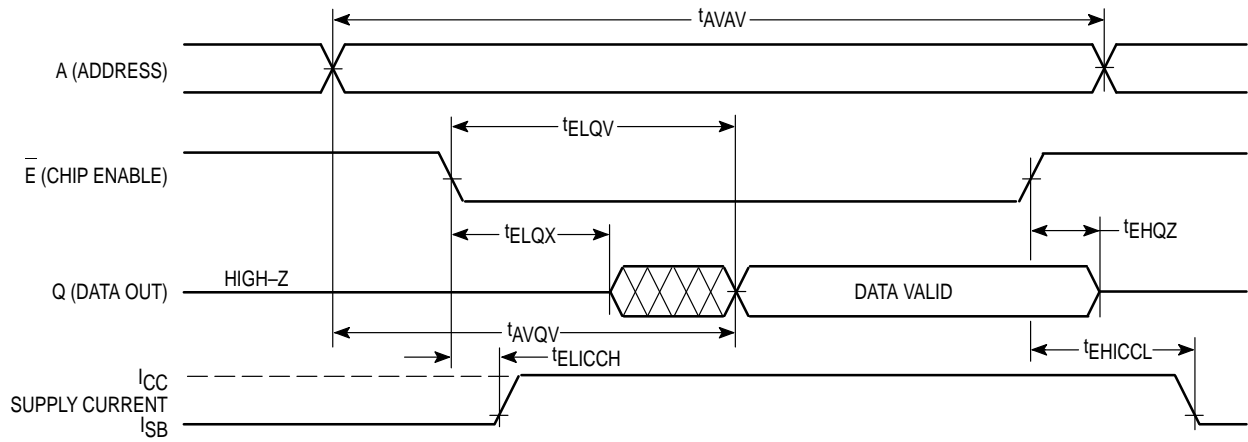
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 4)



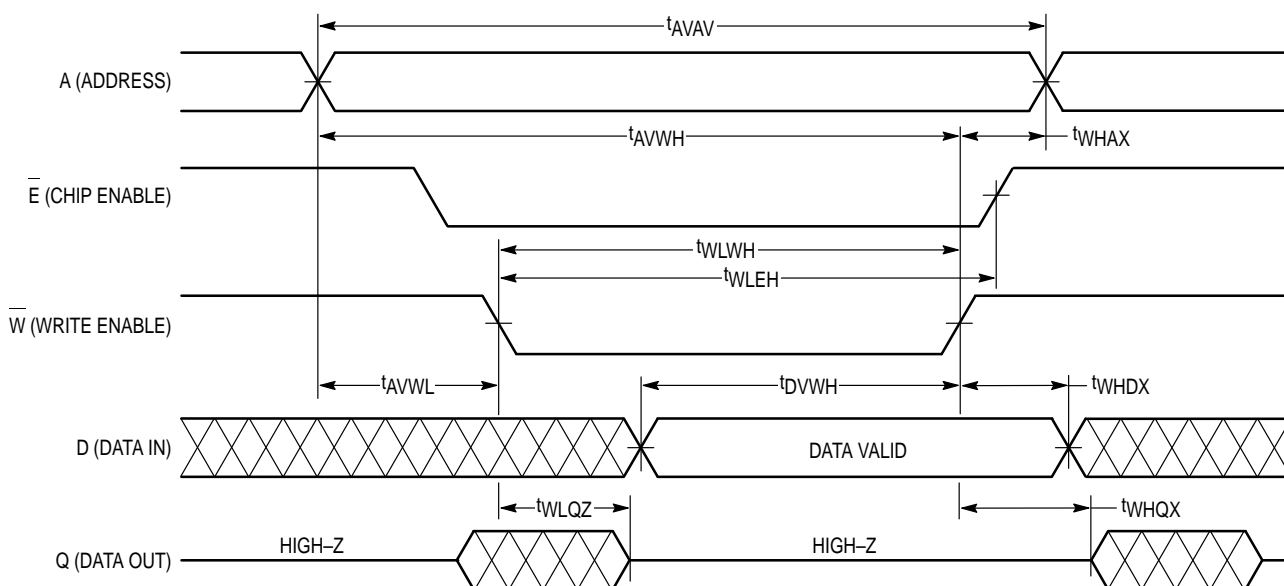
WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM8A10-15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Write Pulse Width	t_{WLWH} , t_{WLEH}	12	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	5	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1b.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 (\overline{W} Controlled See Notes 1 and 2)



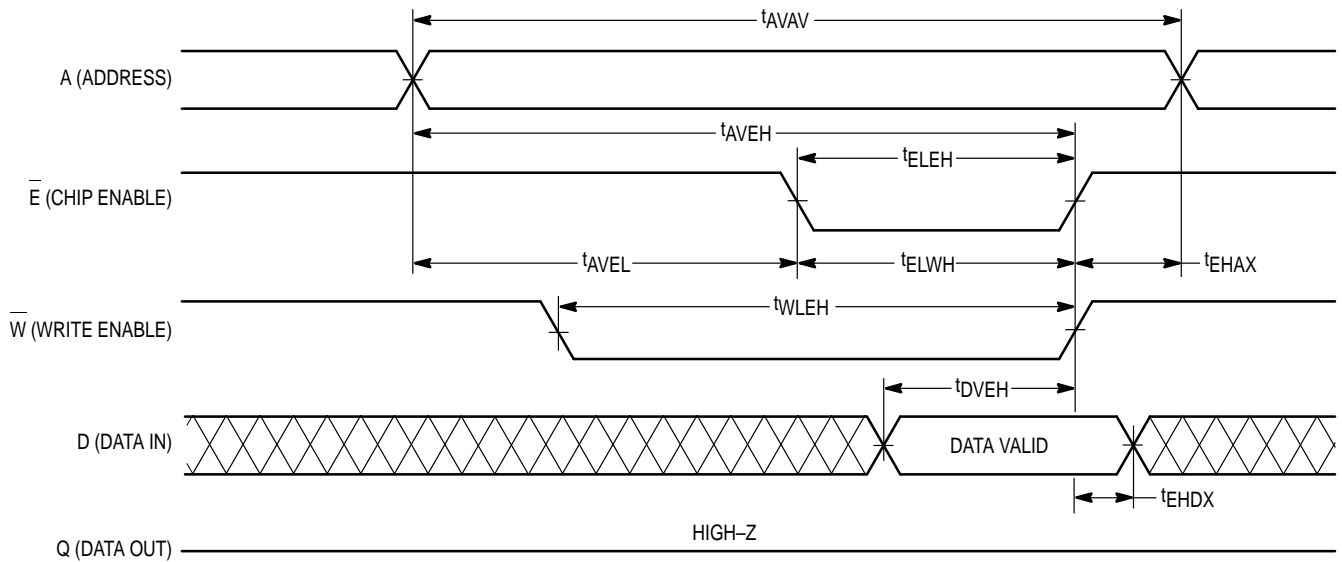
WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM8A10-15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	ns	
Enable to End of Write	t_{ELEH} , t_{ELWH}	10	—	ns	4, 5
Write Pulse Width	t_{WLEH}	12	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	ns	

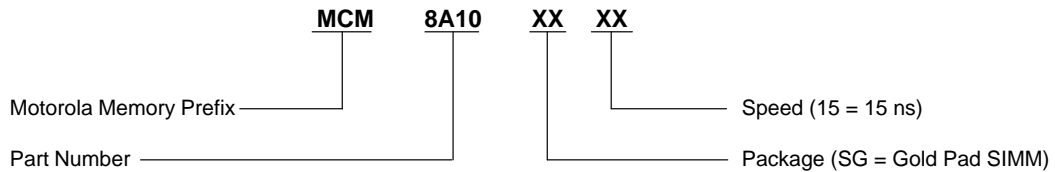
NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high-impedance state.
5. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 (\bar{E} Controlled See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)




Full Part Number — MCM8A10SG15

PACKAGE DIMENSIONS

72-LEAD SIMM

CASE TBD

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MCM8A10/D

