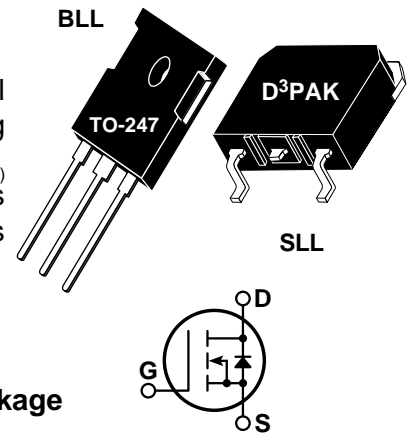


**POWER MOS 7™**

Power MOS 7™ is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7™ by significantly lowering  $R_{DS(ON)}$  and  $Q_g$ . Power MOS 7™ combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge,  $Q_g$
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D<sup>3</sup>PAK Package


**MAXIMUM RATINGS**

 All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	APT8052	UNIT
$V_{DSS}$	Drain-Source Voltage	800	Volts
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	15	Amps
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	60	
$V_{GS}$	Gate-Source Voltage Continuous	±30	Volts
$V_{GSM}$	Gate-Source Voltage Transient	±40	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	295	Watts
	Linear Derating Factor	2.36	W/°C
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	°C
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive and Non-Repetitive)	15	Amps
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	30	mJ
$E_{AS}$	Single Pulse Avalanche Energy <sup>④</sup>	1210	

**STATIC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0V, I_D = 250\mu\text{A}$ )	800			Volts
$I_{D(on)}$	On State Drain Current <sup>②</sup> ( $V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$ )	15			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance <sup>②</sup> ( $V_{GS} = 10V, 0.5 I_{D[Cont.]}$ )			0.52	Ohms
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = V_{DSS}, V_{GS} = 0V$ )			100	μA
	Zero Gate Voltage Drain Current ( $V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$ )			500	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 30V, V_{DS} = 0V$ )			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1\text{mA}$ )	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

**DYNAMIC CHARACTERISTICS**

**APT8052 BLL - SLL**

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
$C_{iss}$	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		2040		pF
$C_{oss}$	Output Capacitance			390		
$C_{rss}$	Reverse Transfer Capacitance			65		
$Q_g$	Total Gate Charge <sup>③</sup>	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$		75		nC
$Q_{gs}$	Gate-Source Charge			10		
$Q_{gd}$	Gate-Drain ("Miller") Charge			43		
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$ $R_G = 1.6\Omega$		13		ns
$t_r$	Rise Time			12		
$t_{d(off)}$	Turn-off Delay Time			52		
$t_f$	Fall Time			15		

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$I_S$	Continuous Source Current (Body Diode)			15	Amps
$I_{SM}$	Pulsed Source Current <sup>①</sup> (Body Diode)			60	
$V_{SD}$	Diode Forward Voltage <sup>②</sup> ( $V_{GS} = 0V, I_S = -I_{D[Cont.]}$ )			1.3	Volts
$t_{rr}$	Reverse Recovery Time ( $I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$ )		650		ns
$Q_{rr}$	Reverse Recovery Charge ( $I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$ )		9.0		$\mu C$
$dv/dt$	Peak Diode Recovery $dv/dt$ <sup>⑤</sup>			10	V/ns

**THERMAL CHARACTERISTICS**

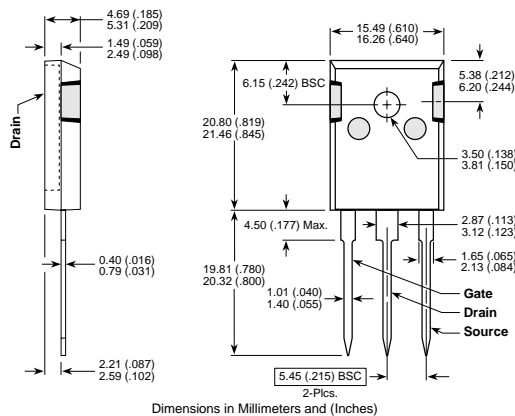
Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.42	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Pulse Test: Pulse width < 380  $\mu s$ , Duty Cycle < 2%

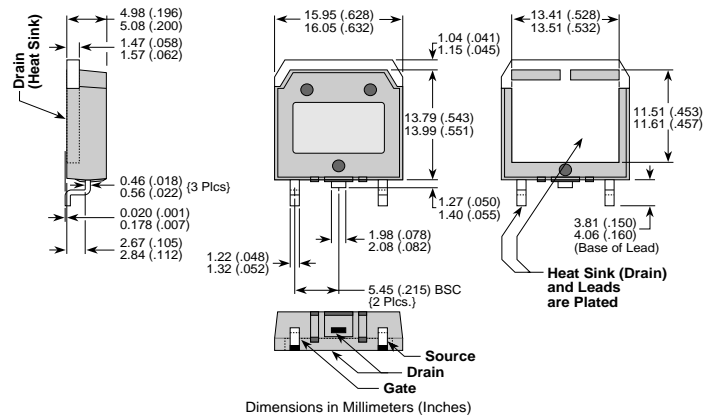
- ③ See MIL-STD-750 Method 3471
- ④ Starting  $T_j = +25^\circ C$ ,  $L = 10.75mH$ ,  $R_G = 25\Omega$ , Peak  $I_L = 15A$
- ⑤  $dv/dt$  numbers reflect the limitations of the test circuit rather than the device itself.  $I_S \leq -I_{D[Cont.]}$ ,  $di_S/dt \leq 700A/\mu s$ ,  $V_R \leq V_{DSS}$ ,  $T_j \leq 150^\circ C$

APT Reserves the right to change, without notice, the specifications and information contained herein.

**TO-247 Package Outline**



**D<sup>3</sup>PAK Package Outline**



050-7058 Rev - 8-2001

APT's devices are covered by one or more of the following U.S. patents: 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336  
5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058