

## PRELIMINARY CUSTOMERPROCUREMENTSPECIFICATION

## Z89331 OTPDIGITAL TELEVISIONCONTROLLER

#### **FEATURES**

| n | Part             | ROM  | RAM*    | Speed |  |  |
|---|------------------|------|---------|-------|--|--|
|   | Number           | (KB) | (Bytes) | (MHz) |  |  |
|   | Z89331           | 24   | 640     | 12    |  |  |
|   | *General-Purpose |      |         |       |  |  |

- n 42-Pin SDIP Package
- n 4.75- to 5.25-Volt Operating Range
- n 0°C to +70°C Temperature Range
- n One-Time Programmable

- n Serial Interfacing I2C Port
- n Fully Customized Character Set
- n Character-Control and Closed-Caption Modes
- n Keypad User Control
- n TV Tuner Serial Interface
- n Direct Video Signals
- n Low-EMI Option

#### GENERAL DESCRIPTION

The Z89331 One-Time Programmable (OTP) Digital Television Controller is designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The Z89331 features a Z89C00 RISC processor core that controls on-board peripheral functions and registers using the standard processor instruction set.

Character attributes can be controlled through two modes: the on-screen display Character-Control Mode and the Closed-Caption Mode. The Character-Control Mode provides access to the full set of attribute controls, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes. Closed-caption text can be decoded directly from the composite video signal and displayed on-screen with the assistance of the processor's digital signal processing (DSP) capabilities.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tunning adjustments, may be accessed through the industry-standard I<sup>2</sup>C port.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

#### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

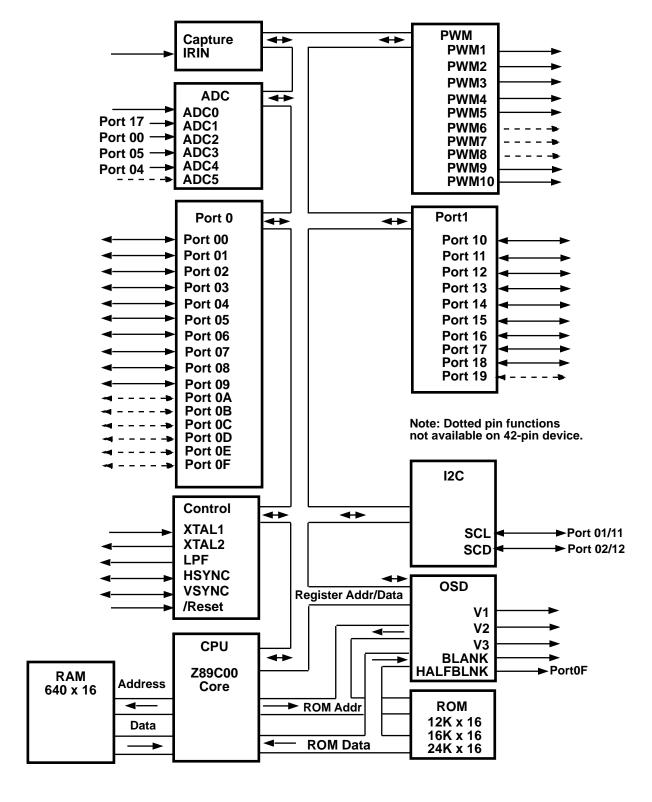
Power connections follow conventional descriptions below:

| Connection      | Circuit                | Device   |
|-----------------|------------------------|--|
| Power<br>Ground | V <sub>cc</sub><br>GND | $egin{array}{c} egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}{c} \egin{array}$ |

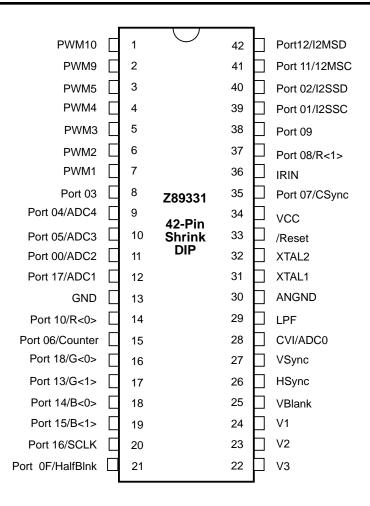
CP95TEL1400 11/95 1



### **GENERAL DESCRIPTION** (Continued)



**Functional Block Diagram** 



42-Pin Shrink DIP Pin Configuration



### **PIN DESCRIPTIONS**

Z89331

| Pin<br>Name             | Function   | Z89331<br>42-Pin SDIP | Config<br>Direction | juration<br>Reset |
|-------------------------|--|-----------------------|---------------------|-------------------|
| V <sub>cc</sub>         | +5 V   | 34                    | PWR                 | PWR               |
| GND                     | 0 V  | 13,30                 | PWR                 | PWR               |
| IRIN                    | Infrared Remote Capture Input                        | 36                    | I                   | I                 |
| ADC[5:0] <sup>a</sup>   | 4-Bit Analog to Digital Converter Input <sup>b</sup> | -,9,10,11,12,2,8      | AI                  | I                 |
| PWM9                    | 14-Bit Pulse Width Modulator<br>Output               | 1,2                   | OD                  | О                 |
| PWM[8:1] <sup>c</sup>   | 8-Bit Pulse Width Modulator                          | -,-,-,3,4             | OD                  | OD                |
|                         | Output   | 5,6,7                 |                     |                   |
| Port0[F:0]d             | Bit Programmable                                     | 21,-,-,-,-,           | В                   | I                 |
|                         | Input/Output Ports                                   | 38,37,35,-,-,         |                     |                   |
|                         |  | 15,8,40,39,11         |                     |                   |
| Port1[9:0] <sup>e</sup> | Bit Programmable                                     | -,16,12,20,           | В                   | I                 |
|                         | Input/Output Ports                                   | 19,18,17,42,          |                     |                   |
|                         |  | 41,14                 |                     |                   |
| MSSCL <sup>f</sup>      | I <sup>2</sup> C Clock I/O                           | 41                    | BOD                 |                   |
| MSSCD <sup>g</sup>      | I <sup>2</sup> C Data I/O                            | 42                    | BOD                 | I                 |
| $SSCL^h$                | I <sup>2</sup> C Clock I/O                           | 39                    | BOD                 | I                 |
| SSCD <sup>i</sup>       | I <sup>2</sup> C Data I/O                            | 40                    | BOD                 | I                 |
| XTAL1                   | Crystal Oscillator Input                             | 31                    | AI                  | AI                |
| XTAL2                   | Crystal Oscillator Output                            | 32                    | AO                  | AO                |
| LPF                     | Loop Filter  | 29                    | AB                  | AB                |
| HSYNC                   | H_Sync   | 26                    | В                   | I                 |
| VSYNC                   | V_Sync   | 27                    | В                   | I                 |
| /RESET                  | Device Reset   | 33                    | I                   | I                 |
| V[3:1]                  | OSD Video Output                                     | 22,23,24              | 0                   | О                 |
|                         | (Typically Drive B, G, and R Outputs)                |                       |                     | _                 |
| Blank                   | OSD Blank Output                                     | 25                    | O                   | 0                 |
| Half Blank <sup>h</sup> | OSD Half Blank Output                                | 21                    | О                   | I                 |
| RGB Digital             | R[1:0],G[1:0], and B[1:0]                            | 37,14,17,             | О                   | I                 |
| Outputs <sup>i</sup>    | Outputs of the RGB Matrix                            | 16,19,18              |                     |                   |
| $SCLK^k$                | Internal Processor SCLK                              | 20                    | O                   | I                 |

#### Notes:

- c) PWM[8,7] is not available on the 42-pin DIP version.
- d) Port0[F:A] is not available on the 42-pin DIP version.

- e) Port19 is not available on the 42-pin DIP version.
- f) SCL I/O pin is shared with Port01 or Port11.
- g) SCD I/O pin is shared with Port02 or Port12.
- h) Half Blank output is a function shared with Port0F.
- i) Digital RGB outputs and the internal SCLK are shared with Port1[5:0].
- k) Internal processor SCLK is shared with Port16.

a) ADC1 input is shared with Port 17, ADC2 input Pin is shared with Port 00. ADC3 input pin is shared with Port 05 and ADC4 input pin is shared with Port 04.

b) ADC0 and ADC5 have a clamp circuit that facilitates Composite video input.



V1, V2, V3 ANALOG OUTPUT Specifications  $V_{CC} = 5.25 \text{ V}$ 

| V <sub>cc</sub> = 5.25 V | Condition                  | Limit           |  |
|--------------------------|----------------------------|-----------------|--|
| Output Voltage           | Bit = 11                   | 3.9 V +/- 0.3 V |  |
|                          | Bit = 10                   | 3.0 V +/- 0.3 V |  |
|                          | Bit = 01                   | 1.8 V +/- 0.3 V |  |
|                          | Bit = 00                   | 0.6 V +/- 0.3 V |  |
| Settling Time            | 70% of DC Level, 10pf Load | < 50 nsec       |  |

# V1, V2, V3 ANALOG OUTPUT Specifications $V_{CC} = 4.75V$

| V <sub>cc</sub> = 4.75V | Condition                  | Limit           |  |
|-------------------------|----------------------------|-----------------|--|
| Output Voltage          | Bit = 11                   | 3.5 V +/- 0.3 V |  |
|                         | Bit = 10                   | 2.6 V +/- 0.3 V |  |
|                         | Bit = 01                   | 1.6 V +/- 0.3 V |  |
|                         | Bit = 00                   | 0.5 V +/- 0.3 V |  |
| Settling Time           | 70% of DC Level, 10pf Load | < 50 nsec       |  |



DC CHARACTERISTICS  $T_{_{A}}=0^{\circ}C \ to + 70^{\circ}C; \ V_{_{CC}}=+\ 4.75 \ V \ to + 5.25V$ 

| Symbol            | Parameter                            | TA = 0° t<br>Min     | o + 70°C<br>Max             | Typical<br>@ 25°C | Units  | Conditions   |
|-------------------|--------------------------------------|----------------------|-----------------------------|-------------------|--------|--|
| $V_{\mathrm{IL}}$ | Input Voltage Low Input Voltage High | 0<br>0.7 V           | $0.2 \text{ V}_{\text{CC}}$ | 1.48<br>3.0       | V<br>V |  |
| $V_{\text{IH}}$   | 1 0 0                                | 0.7 V <sub>CC</sub>  | $V_{cc}$                    |                   |        |  |
| $V_{_{ m HY}}$    | Schmitt Hysteresis                   | $0.1 V_{CC}$         |                             | 0.8               | V      |  |
| $ m V_{PU}$       | Maximum Pull-Up Volta                | ge                   | 13.2                        |                   | V      | [2]  |
| $V_{OL}$          | Output Voltage Low                   |                      | 0.4                         | 0.16              | V      | $I_{OL} = 1.00 \text{ mA}$                               |
|                   |                                      |                      | 0.4                         | 0.19              | V      | $I_{OL} = mA, [1]$                                       |
|                   |                                      |                      | 0.4                         | 0.19              | V      | $I_{OL} = 0.75 \text{ mA}, [2]$                          |
| V <sub>OH</sub>   | Output Voltage High                  | V <sub>CC</sub> -0.4 |                             | 4.75              | V      | $I_{OH} = -0.75 \text{ mA}$                              |
| $I_{IR}$          | Reset Input Current                  | cc                   | -80                         | -46               | μA     | $V_{RL}^{OR} = 0 \text{ V}$                              |
| I <sub>IL</sub>   | Input Leakage                        | -3.0                 | 3.0                         | 0.01              | μA     | $0 \stackrel{\text{RL}}{\text{V}}, \text{V}_{\text{CC}}$ |
| I <sub>OL</sub>   | Tri-State Leakage                    | -3.0                 | 3.0                         | 0.02              | μA     | $0 \text{ V}, \text{V}_{\text{cc}}^{\text{cc}}$          |

#### Note:

[1] Port 0, 1[2] PWM Open-Drain



#### **Pre-Characterization Product:**

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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Zilog, Inc. 210 East Hacienda Ave. Campbell, CA 95008-6600 Telephone (408) 370-8000 FAX 408 370-8056

Internet: http://www.zilog.com