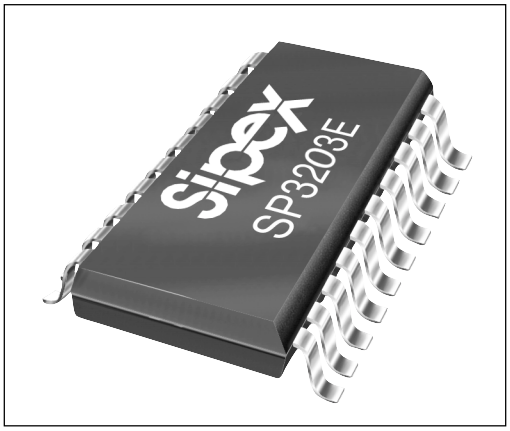
3V RS-232 Serial Transceiver with Logic Selector and15kV ESD Protection

- 3 Driver/ 2 Receiver Architecture
- Logic selector function (V_L) sets TTL input/output levels for mixed logic systems
- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- Minimum 250Kbps data rate under load
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V_{CC} Variations
- Enhanced ESD Specifications:
  - ±15KV Human Body Model
  - ±15KV IEC1000-4-2 Air Discharge
  - ±8KV IEC1000-4-2 Contact Discharge
- Applications
  - Palmtops
  - Cell phone Data Cables
  - PDA's



DESCRIPTION

The SP3203E provides a RS-232 transceiver solution for portable and hand-held applications such as palmtops, PDA's and cell phones. The SP3203E uses an internal high-efficiency, charge-pump that requires only 0.1µF capacitors during 3.3V operation. This charge pump and Sipex's driver architecture allow the SP3203E to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.5V.

The SP3203E is a 3-driver/2-receiver device, with a unique V_L pin to program the TTL input and output logic levels to allow interoperation in mixed-logic voltage systems such as PDA's and cell phones. Receiver outputs will not exceed V_L for V_{OH} and transmitter input logic levels are scaled by the magnitude of the V_L input.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V_+ (NOTE 1).....-0.3V to +7.0V
V_- (NOTE 1).....+0.3V to -7.0V
$V_+ + |V_-|$ (NOTE 1).....+13V
I_{CC} (DC V_{CC} or current)..... ±100mA
Input Voltages
TxIN, $\overline{\text{SHUTDOWN}}$ = GND.....-0.3V to +6.0V
RxIN.....±25V

Output Voltages
TxOUT.....±13.2V
RxOUT.....-0.3V to (V_L + 0.3V)
Short-Circuit Duration
TxOUT.....Continuous
Storage Temperature.....-65°C to +150°C
Power Dissipation per Packages
20-Pin TSSOP
(derate 7.0mW/°C above+70°C).....560mW

NOTE 1: V_+ and V_- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

SPECIFICATIONS

(V_{CC} = V_L = +3V to +5.5V, C1-C4 = 0.1uF, tested at +3.3V ±10%, C1 = 0.047uF, C2-C4 = 0.33uF, tested at +5.0V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = V_L +3.3V, T_A = +25°C.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
DC CHARACTERISTICS (V_{CC} = +3.3V or +5V, T_A = +25°C)						
Supply Current		0.3	1	mA	$\overline{\text{Shutdown}}$ = V_{CC}, no load	
Shutdown Supply Current		1	10	µA	$\overline{\text{Shutdown}}$ = GND	
LOGIC INPUTS						
Input Logic Threshold Low			0.8	V	TxIN, $\overline{\text{Shutdown}}$	V_L = 3.3V or 5.0V
			0.6			V_L = 2.5V
Input Logic Threshold High	2.4			V	TxIN, $\overline{\text{Shutdown}}$	V_L = 5.0V
	2.0					V_L = 3.3V
	1.4					V_L = 2.5V
		0.9				V_L = 1.8V
Transmitter Input Hystersis		0.5		V		
Input Leakage Current		±0.01	±1	µA	TxIN, $\overline{\text{Shutdown}}$	
RECEIVER OUTPUTS						
Output Leakage Currents		±0.05	±10	µA	RxOUT, receivers disabled	
Output Voltage Low			0.4	V	I_{OUT} = 1.6mA	
Output Voltage High	V_L - 0.6	V_L - 0.1		V	I_{OUT} = -1mA	

SPECIFICATIONS (continued)

(V_{CC} = V_L = +3V to +5.5V, C1-C4 = 0.1uF, tested at +3.3V ±10%, C1 = 0.047uF, C2-C4 = 0.33uF, tested at +5.0V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = V_L +3.3V, T_A = +25°C.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
RECEIVER INPUTS						
Input Voltage Range	-25		+25	V		
Input Threshold Low	0.8	1.5		V	T_A = +25°C	V_L = 5.0V
	0.6	1.2				V_L = 2.5V or 3.3V
Input Threshold High		1.8	2.4	V	T_A = +25°C	V_L = 5.0V
		1.5	2.4			V_L = 2.5V or 3.3V
Input Hysteresis		0.5		V		
Input Resistance	3	5	7	kΩ	T_A = +25°C	
TRANSMITTER OUTPUTS						
Output Voltage Swing	±5	±5.4		V	All transmitter outputs loaded with 3kohm to GND. T_A=25°C	
Output Resistance	300	10M		Ω	V_{CC} = V+ = V- = 0, transmitter output = ±2V	
Output Short-Circuit Current			±60	mA	V_{TxOUT} = 0	
Output Leakage Current			±25	µA	V_{TxOUT} = ±12, transmitter disabled; V_{CC} = 0 or 3.0V to 5.5V	
ESD PROTECTION						
R_XIN, T_XOUT ESD Protection		±15		kV	Human Body Model	
		±15			IEC 1000-4-2 Air Gap Discharge	
		±8			IEC 1000-4-2 Contact Discharge	

SPECIFICATIONS (continued)

(V_{CC} = V_L = +3V to +5.5V, C1-C4 = 0.1uF, tested at +3.3V ±10%, C1 = 0.047uF, C2-C4 = 0.33uF, tested at +5.0V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = V_L +3.3V, T_A = +25°C.)

PARAMETER		MIN.	TYP.	MAX.	UNITS	CONDITIONS	
Maximum Data Rate		250			kbps	R_L = 3kΩ, C_L = 1000pF, one transmitter switching	
Receiver Propagation Delay	t_{PHL}		0.15		µs	Receiver input to receiver output C_L =150pF	
	t_{PLH}		0.15				
Receiver Output Enable Time			200		ns	normal operation	
Receiver Output Disable Time			200		ns	normal operation	
Time to Exit Shutdown			100		µs	$IV_{TxOUT}I$ > 3.7V	
Transmitter Skew $It_{PHL} - t_{PLH}I$			100		ns	(Note 2)	
Receiver Skew $It_{PHL} - t_{PLH}I$			50		ns		
Transition-Region Slew Rate		6		30	V/µs	C_L = 150pF to 1000pF	V_{CC} = 3.3V, T_A = +25ºC, R_L = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V
		4		30		C_L = 150pF to 2500pF	

Note 2. Transmitter skew is measured at the transmitter zero crosspoint.

NAME	FUNCTION	PIN NUMBER
		SP3203E
C1+	Positive terminal of the symmetrical charge-pump capacitor, C1.	1
V+	Regulated +5.5V output generated by the charge pump.	2
C1-	Negative terminal of the symmetrical charge-pump capacitor, C1.	3
C2+	Positive terminal of the symmetrical charge-pump capacitor, C2.	4
C2-	Negative terminal of the symmetrical charge-pump capacitor, C2.	5
V-	Regulated -5.5V output generated by the charge pump.	6
R_1IN	RS-232 receiver input.	14
R_2IN	RS-232 receiver input.	13
R_1OUT	TTL/CMOS receiver output.	11
R_2OUT	TTL/CMOS receiver output.	10
T_1IN	TTL/CMOS driver input.	7
T_2IN	TTL/CMOS driver input.	8
T_3IN	TTL/CMOS driver input.	9
T_1OUT	RS-232 driver output.	17
T_2OUT	RS-232 driver output.	16
T_3OUT	RS-232 driver output.	15
GND	Ground.	18
V_{CC}	+3.0V to +5.5V supply voltage.	19
$\overline{\text{SHUTDOWN}}$	Apply logic LOW to shut down drivers and charge pump.	20
V_L	Logic-Level Supply Voltage Selection	12

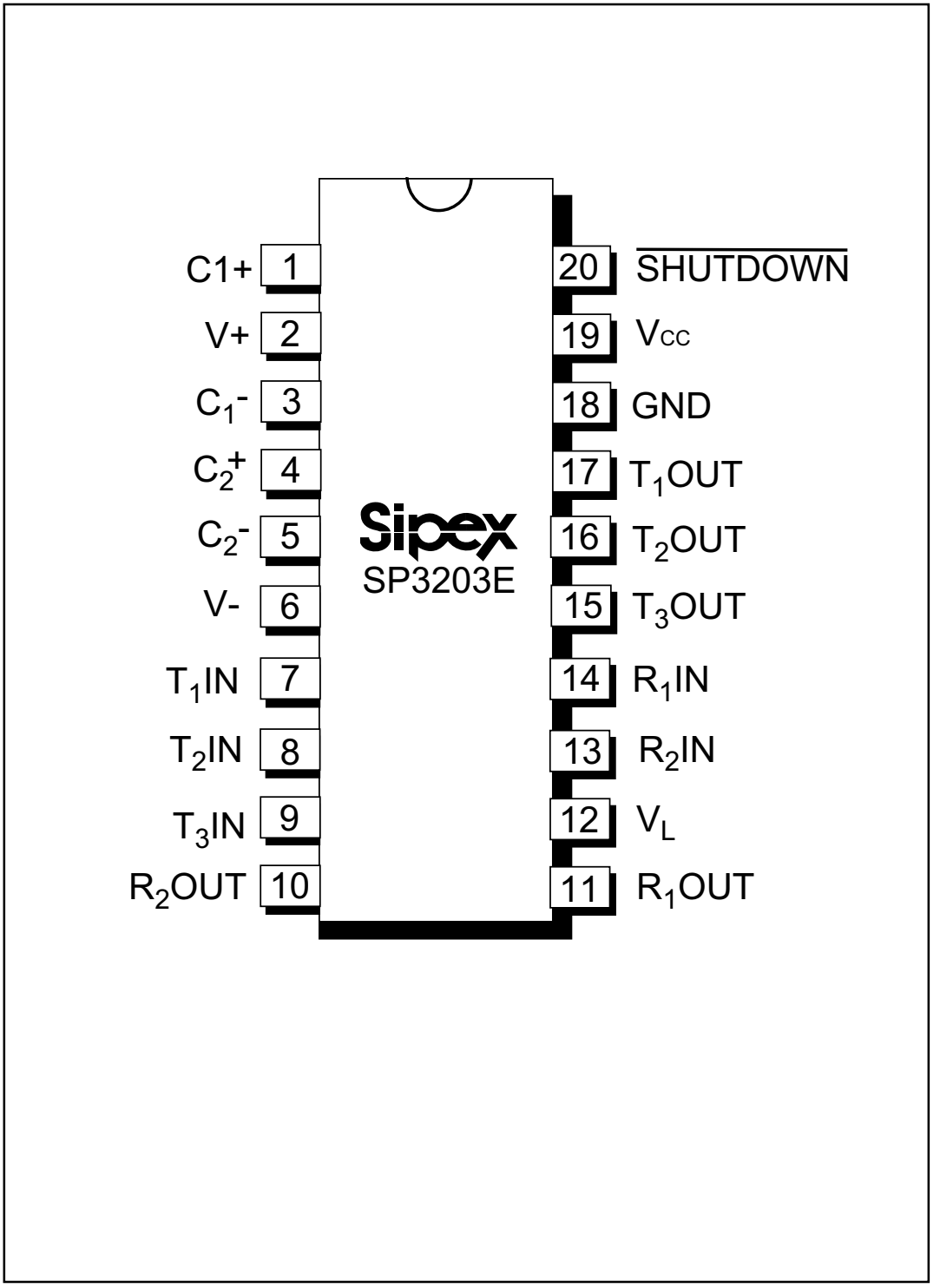


Figure 7. SP3203E Pinout Configuration

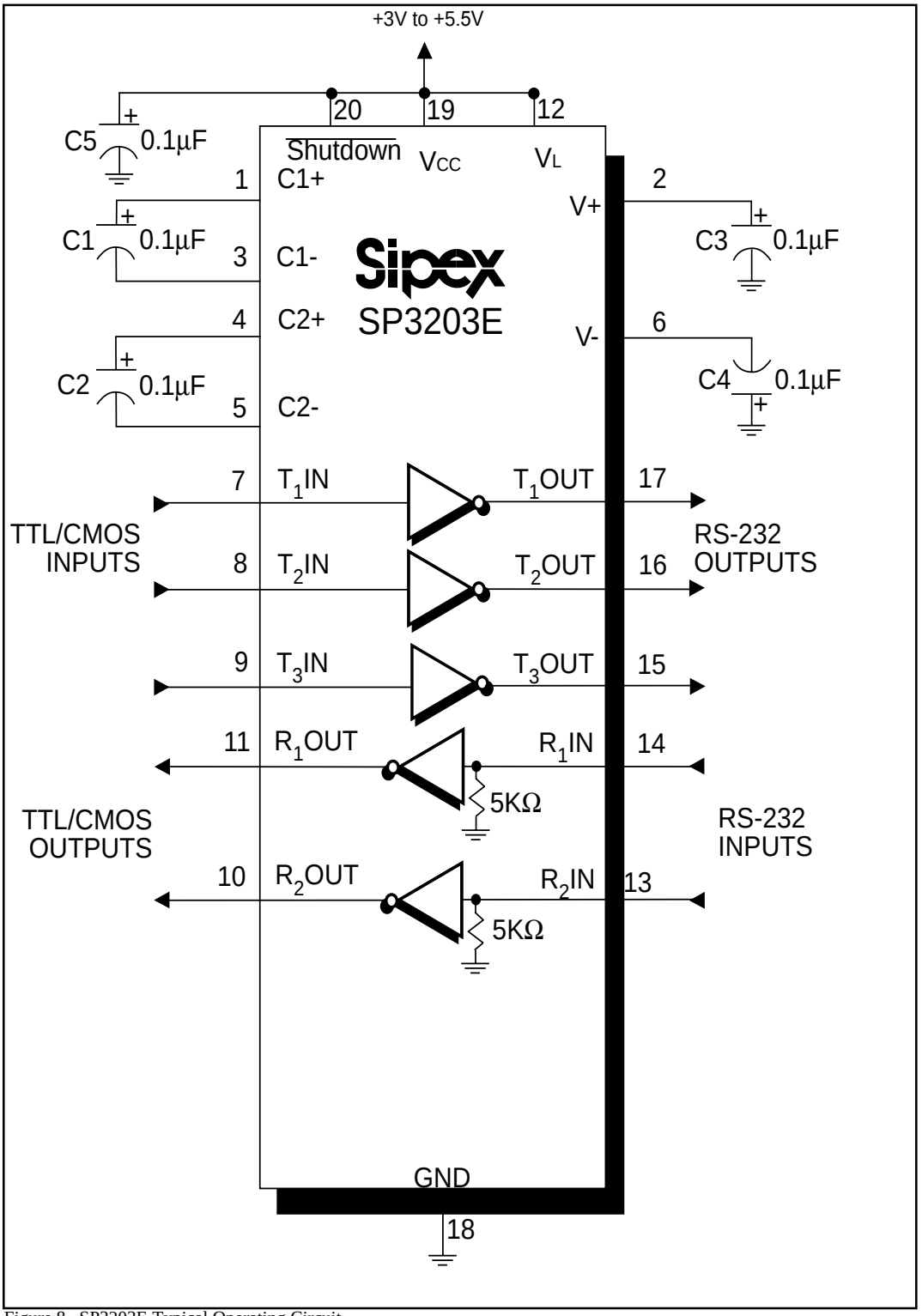


Figure 8. SP3203E Typical Operating Circuit

DESCRIPTION

The SP3203E is a 3-driver/2-receiver device that can be operated as a full duplex, RS-232 serial transceiver with the 3rd driver acting as a control line allowing a Ring Indicator (RI) signal to alert the UART on the PC.

This transceiver meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers, PDA's and cell phones. The SP3203E devices feature Sipex's proprietary and patented (U.S.#5,306,954) on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. The SP3203E devices can operate at a minimum data range of 250kbps, driving a single driver. The SP3203E is a 3-driver/2-receiver device.

THEORY OF OPERATION

The SP3203E contains four basic circuit blocks: 1. drivers, 2. receivers, 3. a Sipex proprietary charge pump and 4. V_L circuitry.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232F and all previous RS-232 versions. The driver output stages are turned off (High Impedance) when the device is in shutdown mode.

The drivers typically can operate at a data rate of 250Kbps. The drivers can guarantee a data rate of 120Kbps fully loaded with 3KΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

The SP3203E driver can maintain high data rates up to 250Kbps with a single driver loaded. Figure 9 shows a loopback test circuit used to test the RS-232 Drivers. Figure 10 shows the test results of the loopback circuit with all three drivers active at 120Kbps with typical RS-232 loads in parallel with 1000pF capacitors. Figure 11 shows the test results where one driver was active at 250Kbps and all three drivers loaded with an RS-232 receiver in parallel with a 1000pF capacitor. The transmitter inputs do not have pull-up resistors. Connect unused inputs to ground or V_L

Receivers

The receivers convert ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers are disabled when in shutdown. The truth table logic of the SP3203E driver and receiver outputs can be found in Table 1.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is immune to noisy transmission lines. Should an input be left unconnected, an internal 5KΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is a Sipex–patented design (U.S. #5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply

DEVICE: SP3203E			
$\overline{\text{SHUTDOWN}}$	T_XOUT	R_XOUT	Charge Pump
0	High-Z	High-Z	Inactive
1	Active	Active	Active

Table 1. $\overline{\text{SHUTDOWN}}$ Truth Table.

(Note: When device in shutdown, the SP3203E's charge pump is turned off and V+ decays to Vcc. V- is pulled to ground and the transmitter outputs are disabled as High Impedance.)

consists of a regulated dual charge pump that provides output voltages of 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a of 5.5V, the charge pump is enabled. If the output voltages exceed a of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting (Figure 12). A description of each phase follows.

V_{SS} Charge Storage-Phase 1(Figure 13)

During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

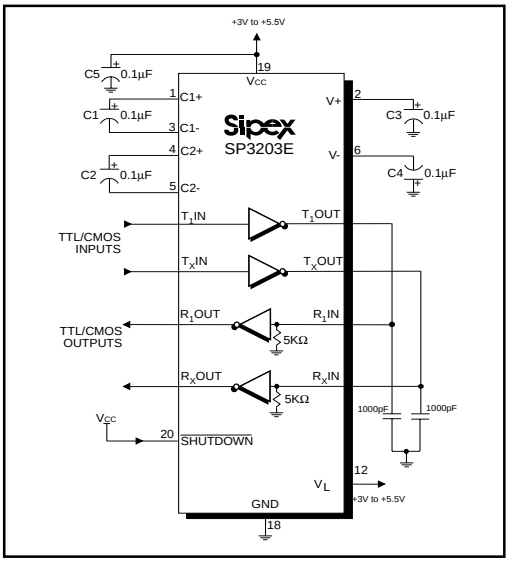


Figure 9. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

V_{SS} Transfer-Phase 2 (Figure 14)

Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

V_{DD} Charge Storage-Phase 3 (Figure 15)

The third phase of the clock is identical to the first phase — the charge transferred in C_1 pro-

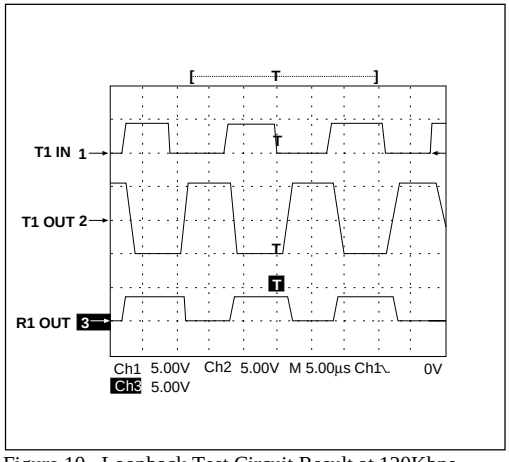


Figure 10. Loopback Test Circuit Result at 120Kbps (All Drivers Fully Loaded)

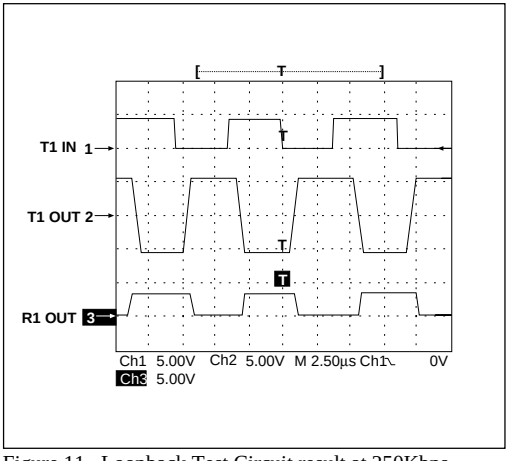


Figure 11. Loopback Test Circuit result at 250Kbps (All Drivers Fully Loaded)

duces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

V_{DD} Transfer-Phase 4 (Figure 16)

The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}, in a no–load condition, V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent ineffiencies in the design.

The clock rate for the charge pump is typically operates at 250kHz. The external capacitors are usually 0.1µF with a 16V breakdown voltage rating.

V_L Supply Level

Current RS-232 serial tranceivers are designed with fixed 5V or 3.3V TTL input/output voltages levels. The V_L function in the SP3203E allows the end user to set the TTL input/output voltage levels independent of V_{CC}. By connecting V_L to the main logic bus of system, the TTL input/output limits and threshold are reset to interface with the on board low voltage logic circuity.

Capacitor Selection Table:		
V_{CC} (V)	C1 (µF)	C2-C4(µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.22	1

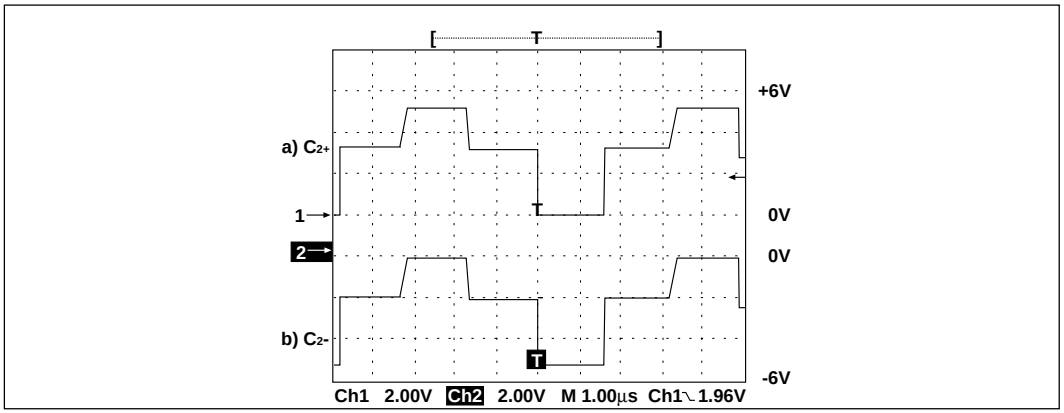


Figure 12. Charge Pump Waveforms

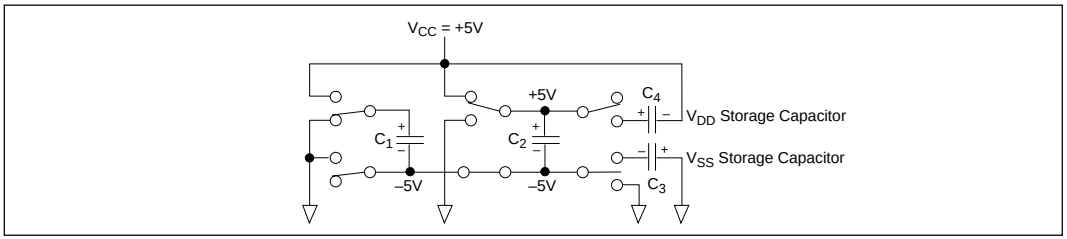


Figure 13. Charge Pump — Phase 4 - V_{SS} Charge Storage

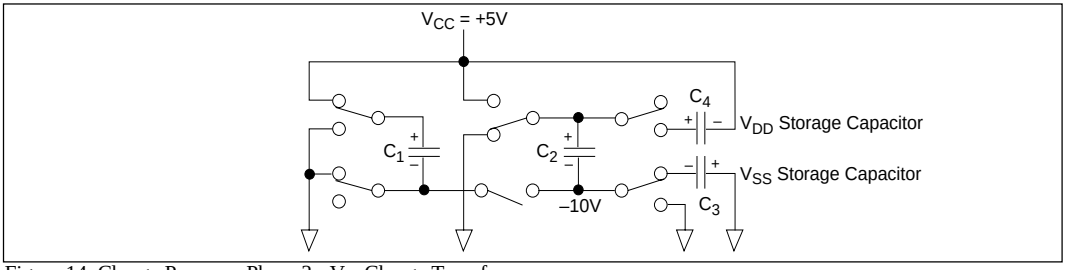


Figure 14. Charge Pump — Phase 3 - V_{SS} Charge Transfer

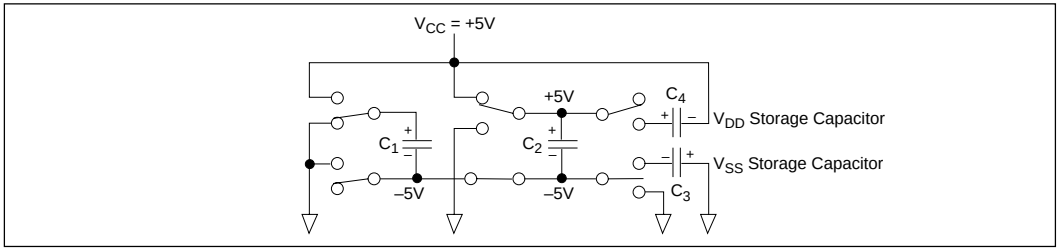


Figure 15. Charge Pump — Phase 2 - V_{DD} Charge Storage

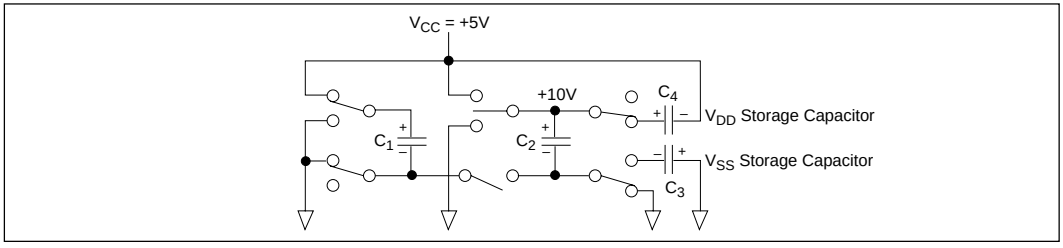


Figure 16. Charge Pump — Phase 1 - V_{DD} Charge Transfer

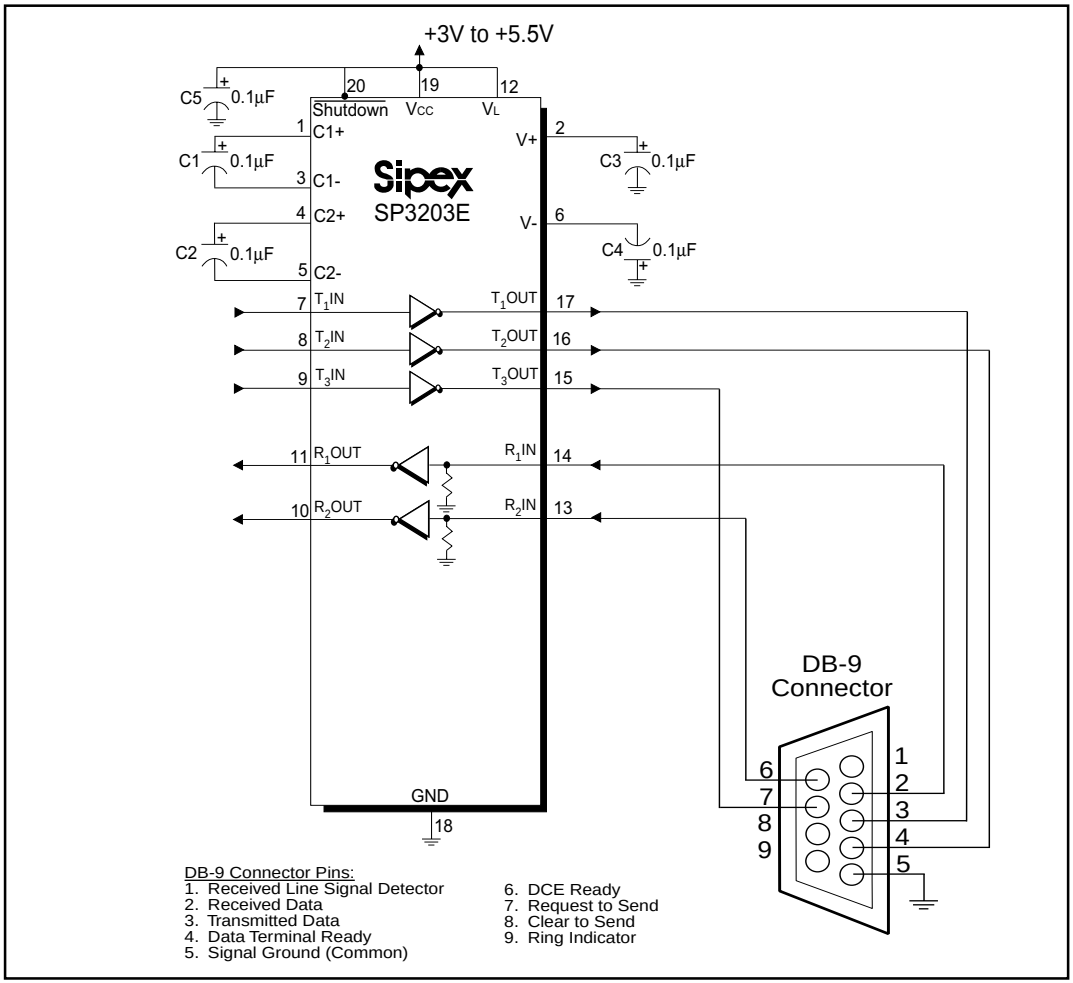


Figure 17. Circuit for the connectivity of the SP3203E with a DB-9 connector

ESD TOLERANCE

The SP3203E incorporates ruggedized ESD cells on all driver output and receiver input pins. The improved ESD tolerance is at least 15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC1000-4-2 Air-Discharge
c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 18. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on Figure 19. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit model in Figures 18 and 19 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC

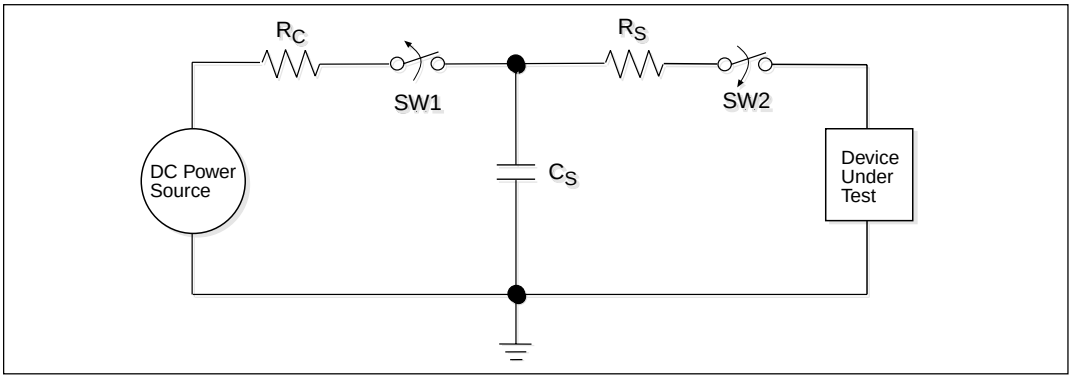


Figure 18. ESD Test Circuit for Human Body Model

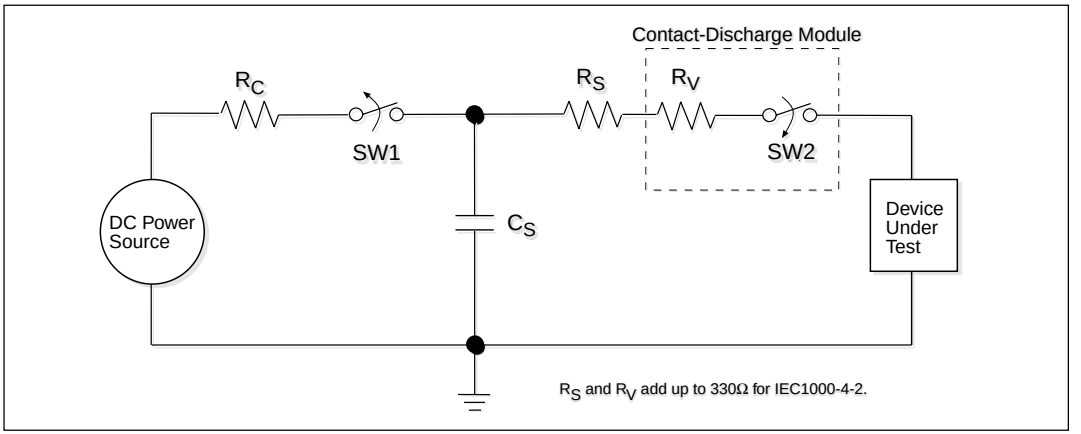


Figure 19. ESD Test Circuit for IEC1000-4-2

power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kW an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330W an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

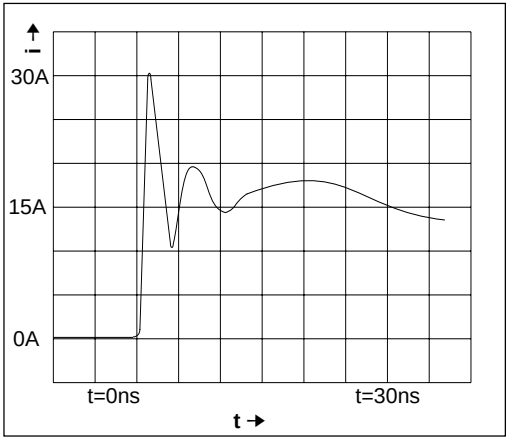
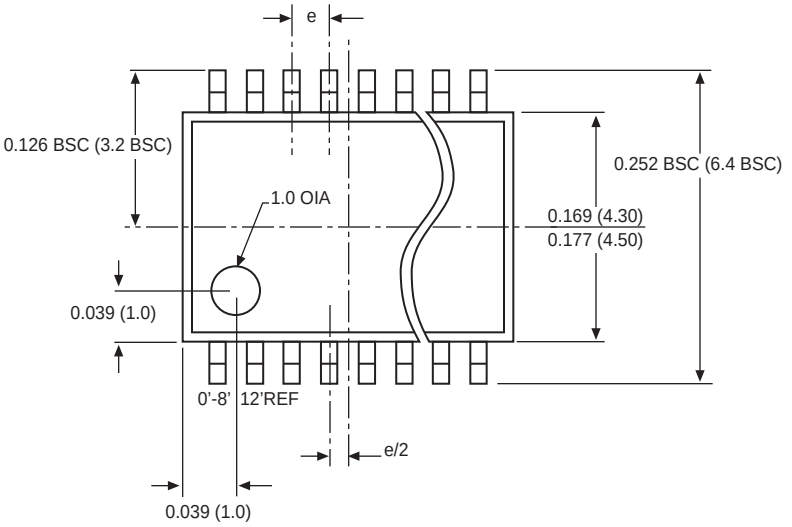


Figure 20. ESD Test Waveform for IEC1000-4-2

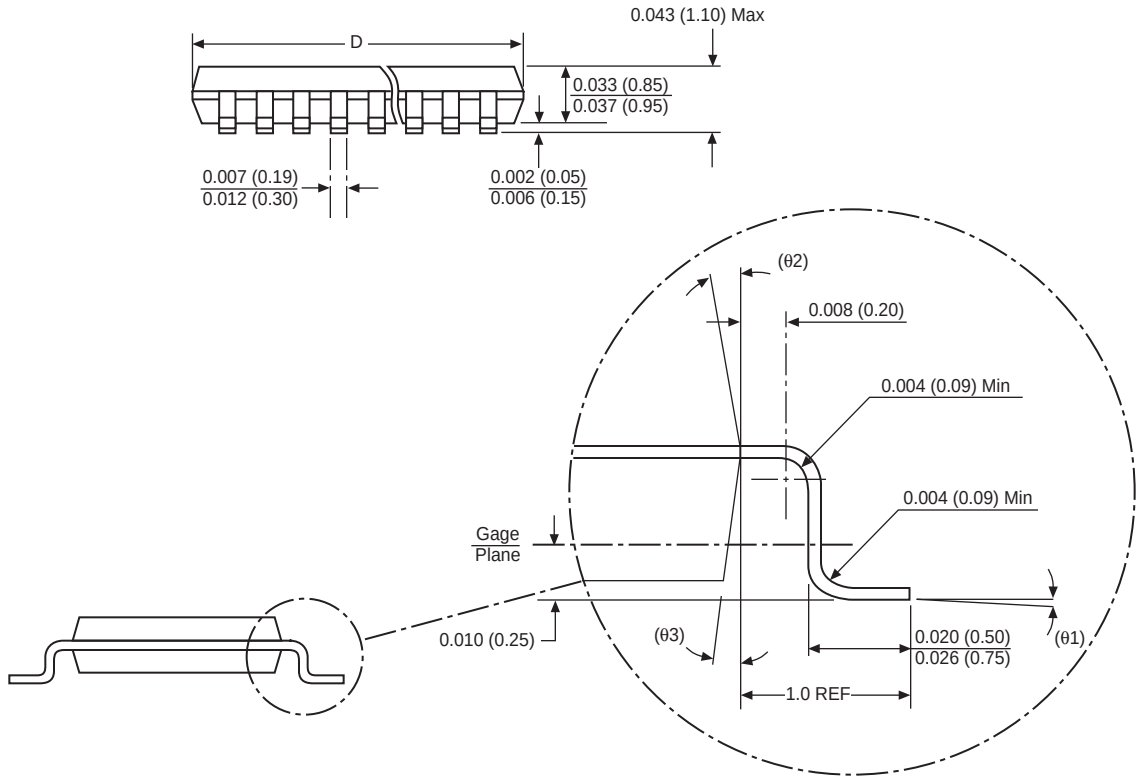
DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

Table 2. Transceiver ESD Tolerance Levels

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)



DIMENSIONS in inches (mm) Minimum/Maximum	
Symbol	**20 Lead**
D	0.252/0.260 (6.40/6.60)
e	0.026 BSC (0.65 BSC)



ORDERING INFORMATION

Model	Temperature Range	Package Types
SP3203ECY	0°C to +70°C	20-pin TSSOP
SP3203EEY	-40°C to +85°C	20-pin TSSOP

Please consult the factory for pricing and availability on a Tape-On-Reel option.

SIGNAL PROCESSING EXCELLENCE

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