



N-Channel 30-V (D-S) MOSFET

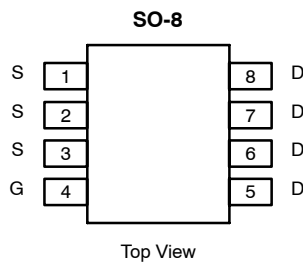
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0135 @ $V_{GS} = 10$ V	10
	0.020 @ $V_{GS} = 4.5$ V	8

FEATURES

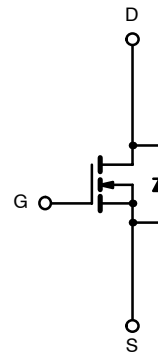
- TrenchFET® Power MOSFET
- 100% R_g Tested

APPLICATIONS

- Battery Switch



Ordering Information: Si4410BDY
Si4410BDY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	10	7.5	A
		$T_A = 70^\circ\text{C}$	8	6	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	50			
Continuous Source Current (Diode Conduction) ^a	I_S	2.3	1.26		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.5	1.4	W
		$T_A = 70^\circ\text{C}$	1.6	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	40	50	$^\circ\text{C}/\text{W}$
		Steady State	70	90	
Maximum Junction-to-Foot (Drain)	R_{thJF}	25	30		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.



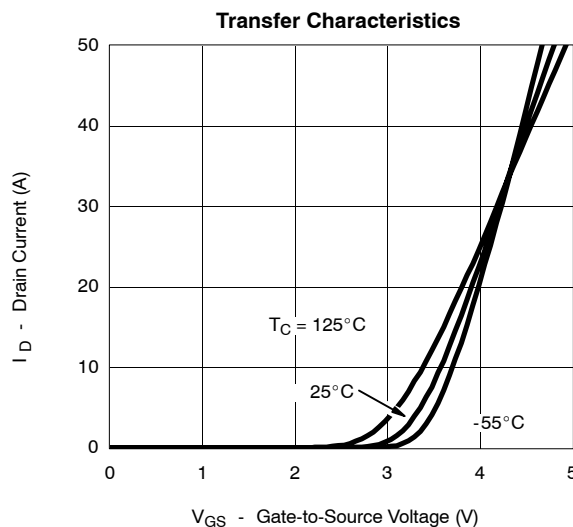
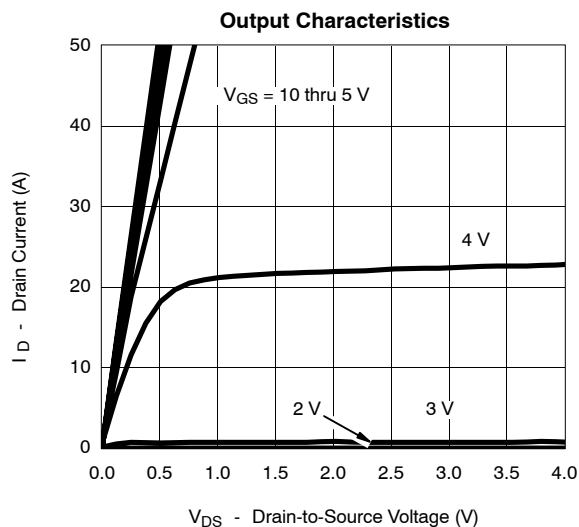
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		3.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 10 A		0.011	0.0135	Ω
		V _{GS} = 4.5 V, I _D = 5 A		0.0165	0.020	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A		25		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.3 A, V _{GS} = 0 V		0.76	1.1	V
Dynamic^b						
Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 5 V, I _D = 10 A		13	20	nC
Total Gate Charge	Q _{gt}	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A		25	40	
Gate-Source Charge	Q _{gs}			5.5		
Gate-Drain Charge	Q _{gd}			3.7		
Gate Resistance	R _g	f = 1 MHz	0.5	1.6	2.7	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, R _L = 25 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		10	15	ns
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			40	60	
Fall Time	t _f			15	25	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 2.3 A, di/dt = 100 A/μs		35	

Notes

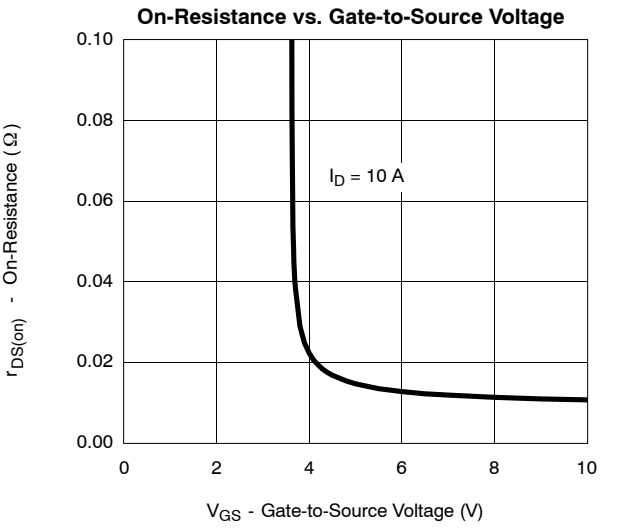
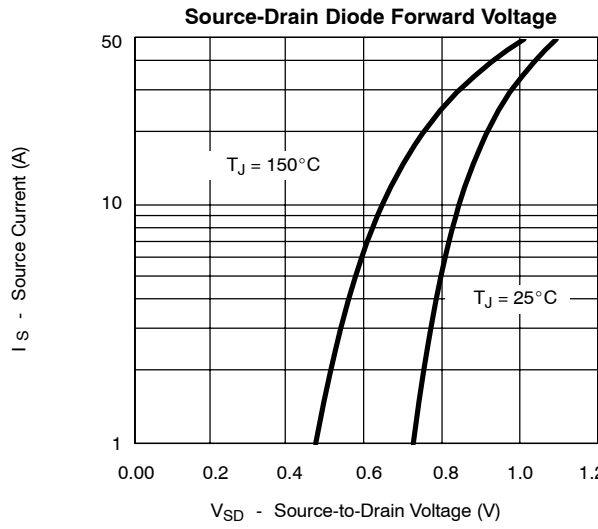
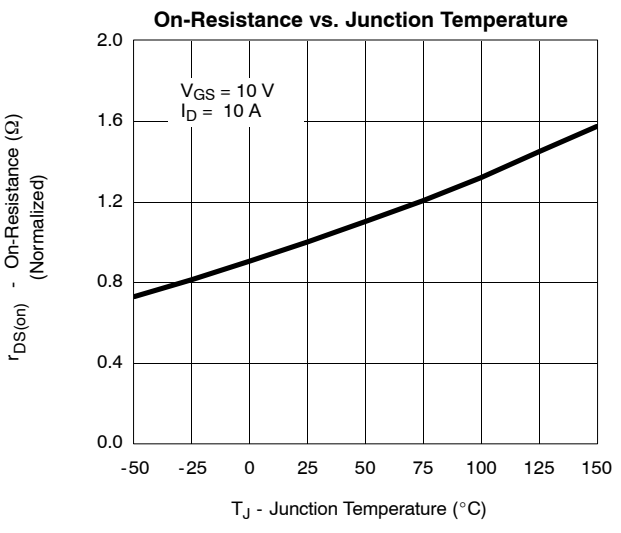
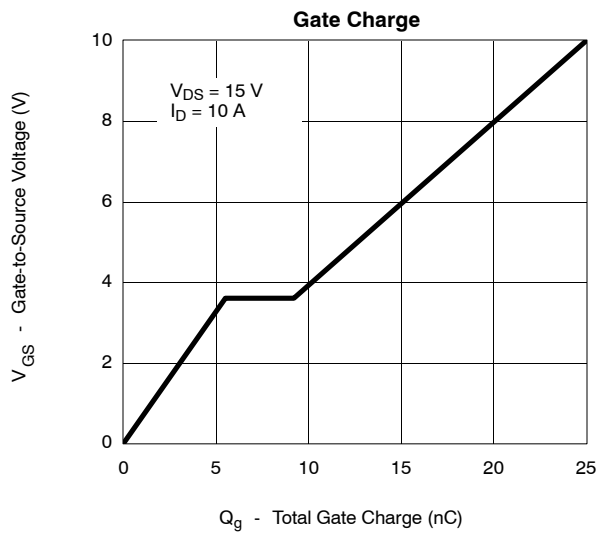
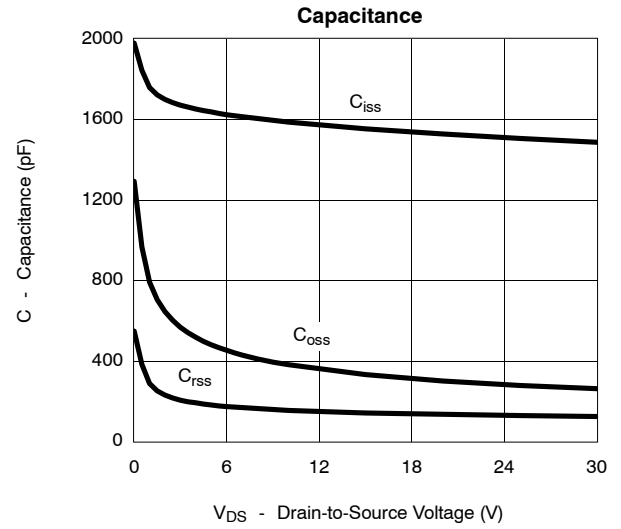
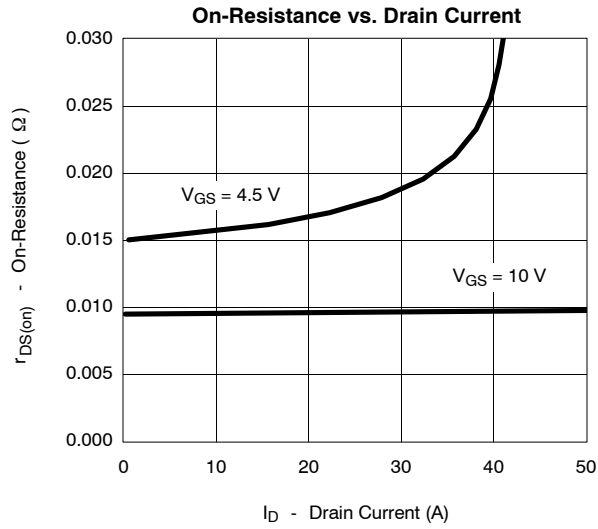
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



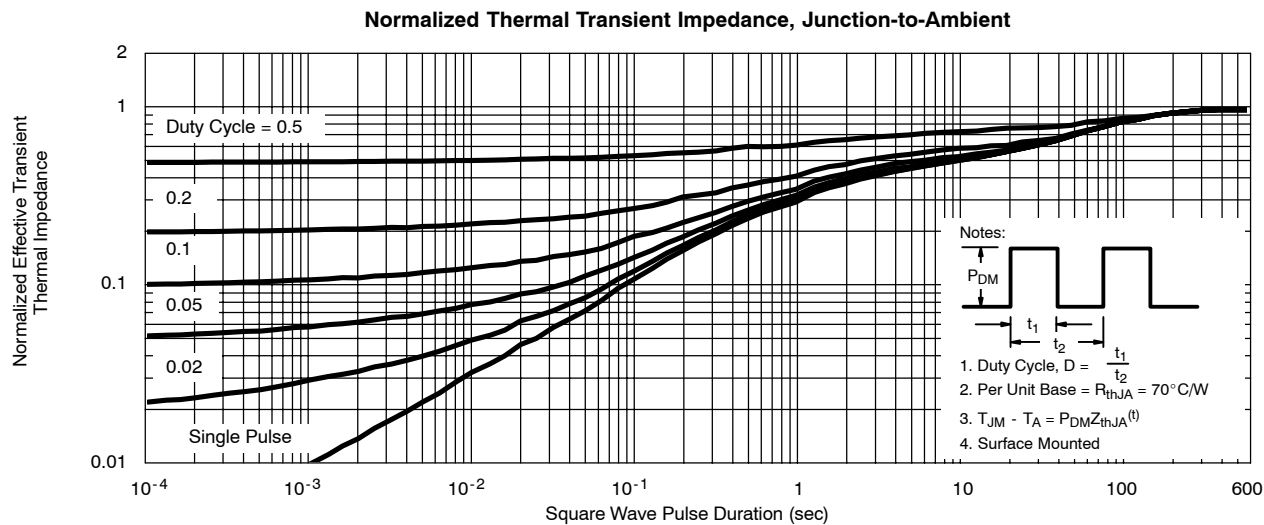
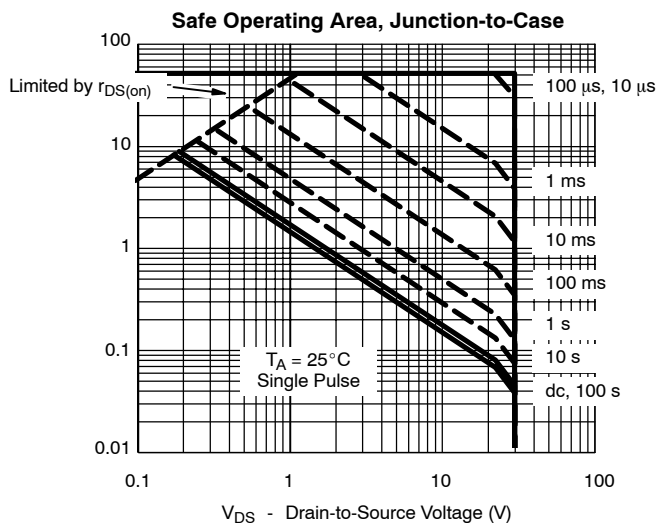
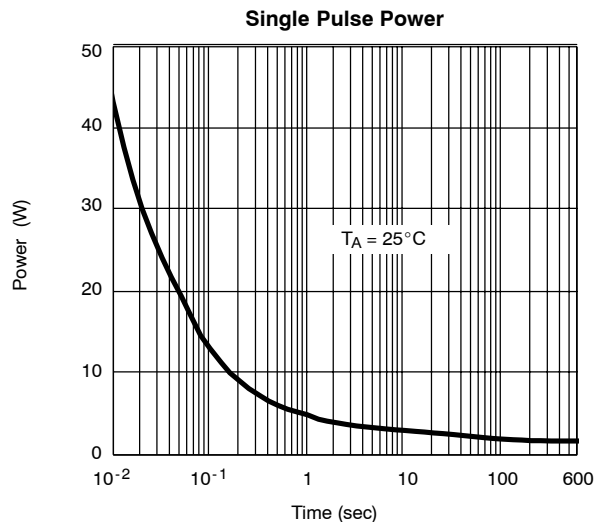
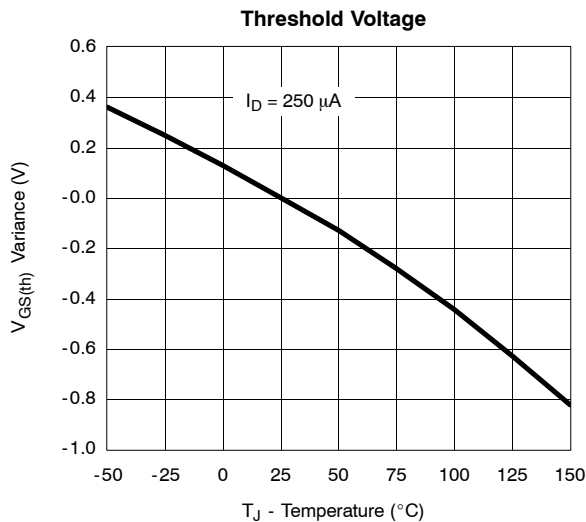


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