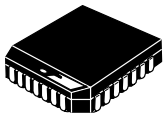
4-Bit Parallel/Serial Converter

MC10E446
MC100E446

4-BIT PARALLEL/ SERIAL CONVERTER

The MC10E/100E446 is an integrated 4-bit parallel to serial data converter. The device is designed to operate for NRZ data rates of up to 1.3Gb/s. The chip generates a divide by 4 and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the parallel data into a serial stream from bit D0 to D3. A serial input is provided to cascade two E446 devices for 8 bit conversion applications. Note that the serial output data clocks off of the negative input clock transition.

- On Chip Clock ÷4 and ÷8
- 1.5 Gb/s Typical Data Rate Capability
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8 Bits
- Internal 75kΩ Input Pulldown Resistors
- Extended 100E V_{EE} Range of -4.2V to -5.46V



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The SYNC input will asynchronously reset the internal clock circuitry. This pin allows the user to reset the internal clock conversion unit and thus select the start of the conversion process.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the mode input is driven HIGH the internal load clock will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E446's. When cascaded in an 8-bit conversion scheme the devices will not operate at the 1.3Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E446.

For lower data rate applications a V_{BB} reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz differential input signals are recommended. For single-ended inputs the V_{BB} pin is tied to the inverting differential input and bypassed via a 0.01µF capacitor. The V_{BB} provides the switching reference for the input differential amplifier. The V_{BB} can also be used to AC couple an input signal, for more information on AC coupling refer to the interfacing section of the design guide in the ECLinPS™ data book.

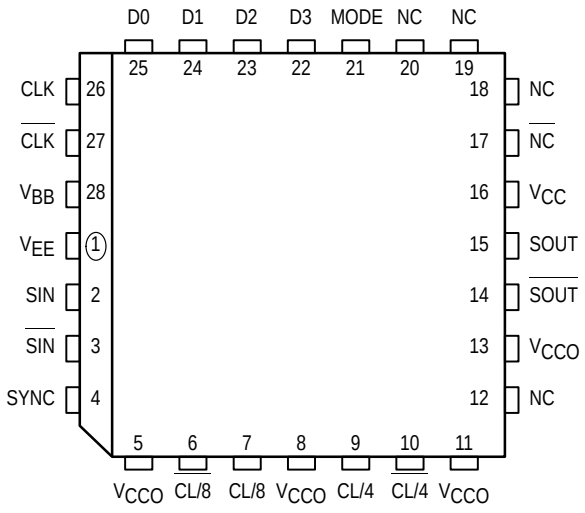
PIN NAMES

Pin	Function
SIN	Differential Serial Data Input
D0 – D3	Parallel Data Inputs
SOUT, $\overline{\text{SOUT}}$	Differential Serial Data Output
CLK, $\overline{\text{CLK}}$	Differential Clock Inputs
CL/4, $\overline{\text{CL/4}}$	Differential ÷4 Clock Output
CL/8, $\overline{\text{CL/8}}$	Differential ÷8 Clock Output
MODE	Conversion Mode 4-Bit/8-Bit
SYNC	Conversion Synchronizing Input

FUNCTION TABLES

Mode	Conversion
L	4-Bit
H	8-Bit

Pinout: 28-Lead PLCC (Top View)



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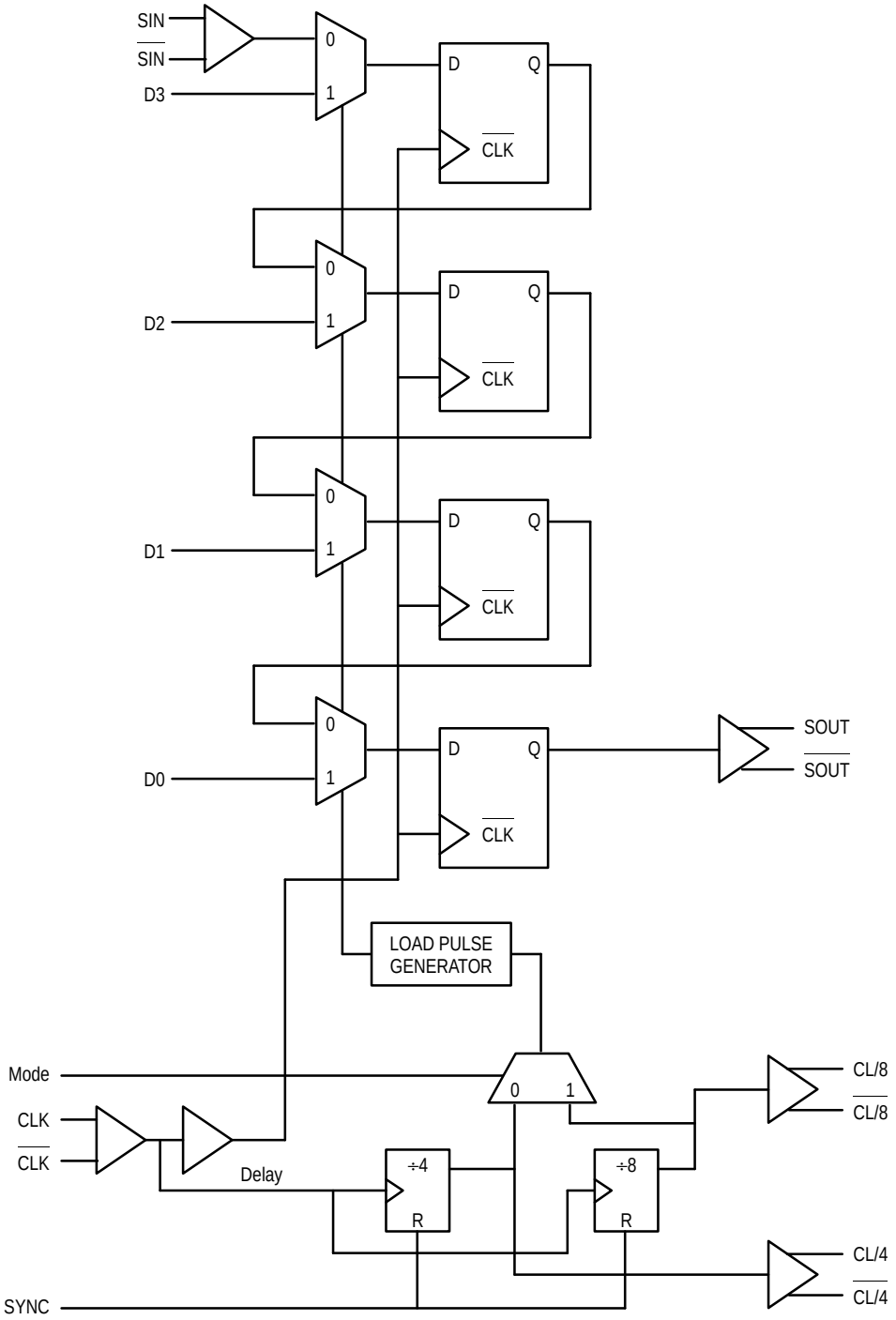
LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = $V_{EE(min)}$ to $V_{EE(max)}$; V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			150			150			150	µA	
V_{OH}	Output HIGH Voltage										V	
	10E (SOUT Only)	–1020		–790	–980		–760	–910		–670		1
	100E (SOUT Only)	–1025		–830	–1025		–830	–1025		–830		1
V_{BB}	Output Reference Voltage 10E	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V	
	100E	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26		
I_{EE}	Power Supply Current 10E		126	151		126	151		126	151	mA	
	100E		126	151		126	151		145	174		

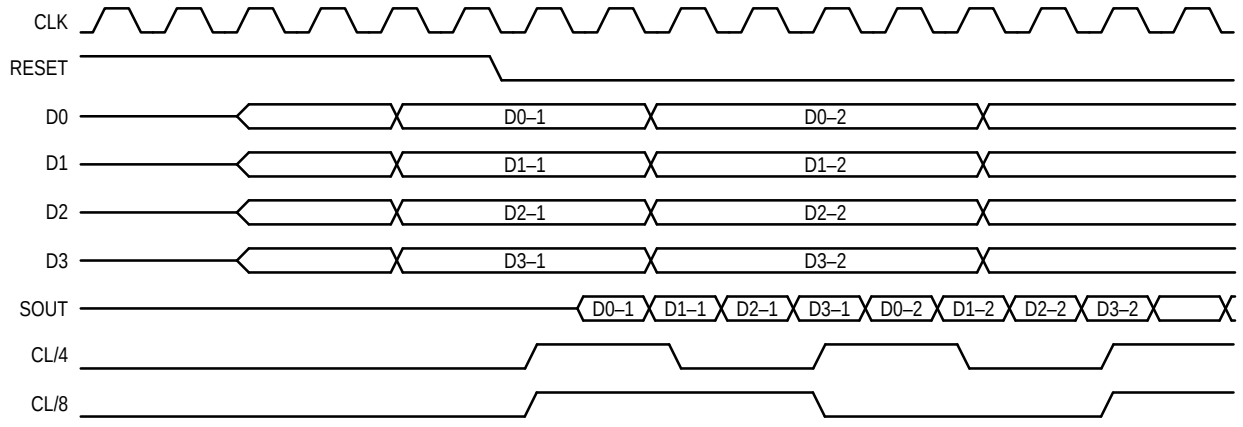
1. The maximum V_{OH} limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E V_{OH} levels.

AC CHARACTERISTICS (V_{EE} = $V_{EE(min)}$ to $V_{EE(max)}$; V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
F_{MAX}	Max Conversion Frequency	1.3	1.6		1.3	1.6		1.3	1.6		Gb/s NRZ	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK to SOUT[1]	1020	1200	1480	1020	1200	1480	1020	1200	1480		
	CLK to CL/4	650	850	1050	650	850	1050	650	850	1050		
	CLK to CL/8	800	1050	1300	800	1050	1300	800	1050	1300		
	SYNC to CL/4, CL/8	650	850	1100	650	850	1100	650	850	1100		
t_S	Setup Time[2] SIN, Dn	-200	-450		-200	–450		–200	–450		ps	
t_h	Hold Time[2] SIN, Dn	900	650		900	650		900	650		ps	
t_{RR}	Reset Recovery Time SYNC	500	300		500	300		500	300		ps	
t_{PW}	Min Pulse Width CLK, MR	300			300			300			ps	
t_r t_f	Rise/Fall Times SOUT	100	225	350	100	225	350	100	225	350	ps	20% - 80%
	Other	200	425	650	200	425	650	200	425	650		

1. Propagation delays measured from negative going clock edge.
2. Relative to negative clock edge.

Timing Diagrams



Timing Diagram A. 4:1 Parallel to Serial Conversion

Applications Information

The MC10E/100E446 is an integrated 4:1 parallel to serial converter. The chip is designed to work with the E445 device to provide both transmission and receiving of a high speed serial data path. The E446 can convert 4 bits of data into a 1.3Gb/s NRZ data stream. The device features a SYNC input which allows the user to reset the internal clock circuitry and restart the conversion sequence (see timing diagram A).

The E446 features a differential serial input and internal divide by 8 circuitry to facilitate the cascading of two devices to build a 8:1 multiplexer. Figure 1 illustrates the architecture for a 8:1 multiplexer using two E446's; the timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock to serial output propagation delay plus the setup time of the serial input pins must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, TPD CLK to SOUT = 1480ps and tS for SIN = –200ps, yields a minimum period of 1280ps or a clock frequency of 780MHz.

The clock frequency is somewhat lower than that of a single converter, to increase this frequency some games can be played with the clock input of the higher order E446. By delaying the clock feeding E446A relative to the clock of E446B the frequency of operation can be increased.

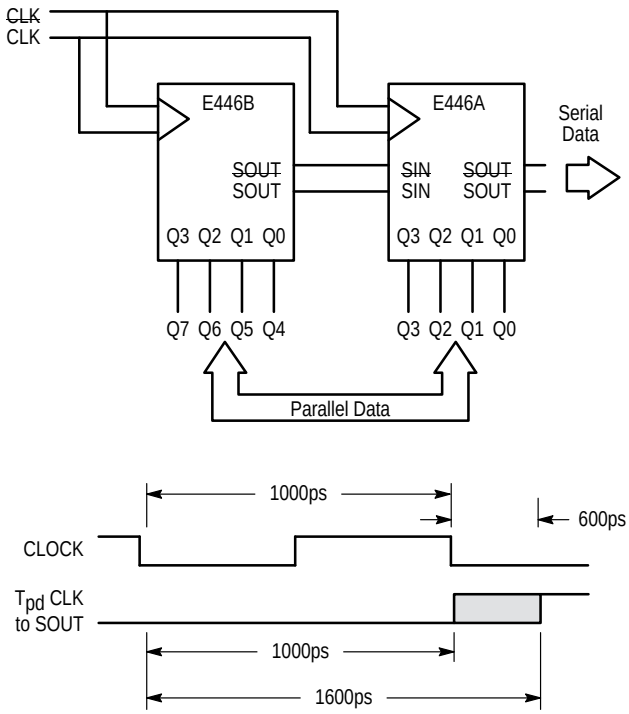
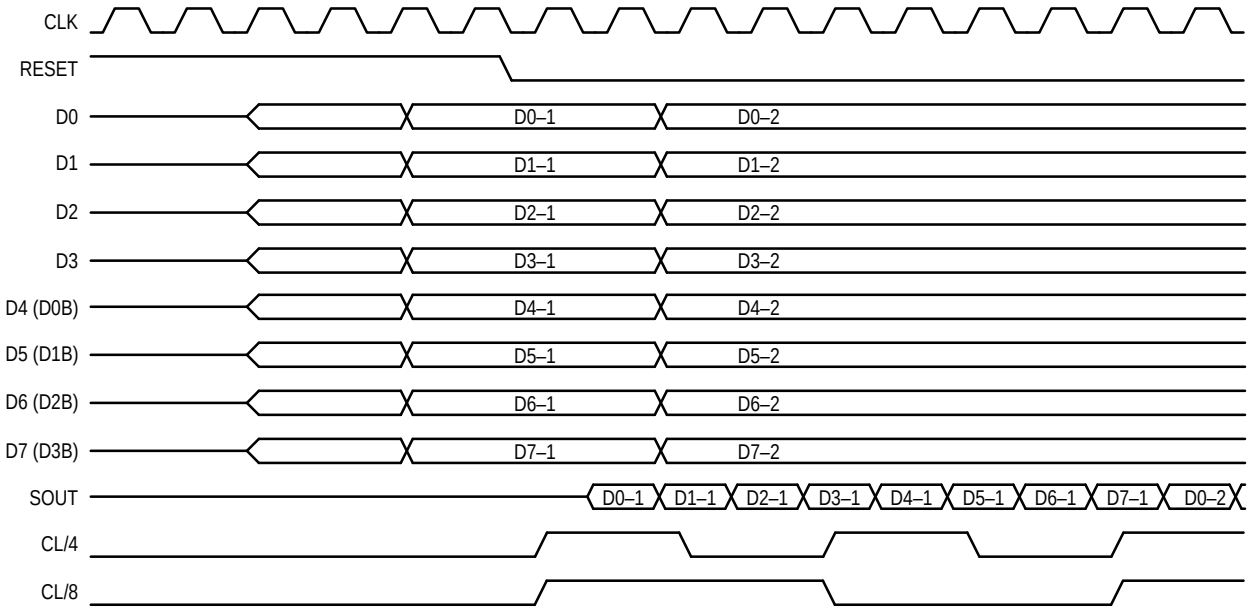


Figure 1. Cascaded 8:1 Converter Architecture



Timing Diagram B. 8:1 Parallel to Serial Conversion

OUTLINE DIMENSIONS

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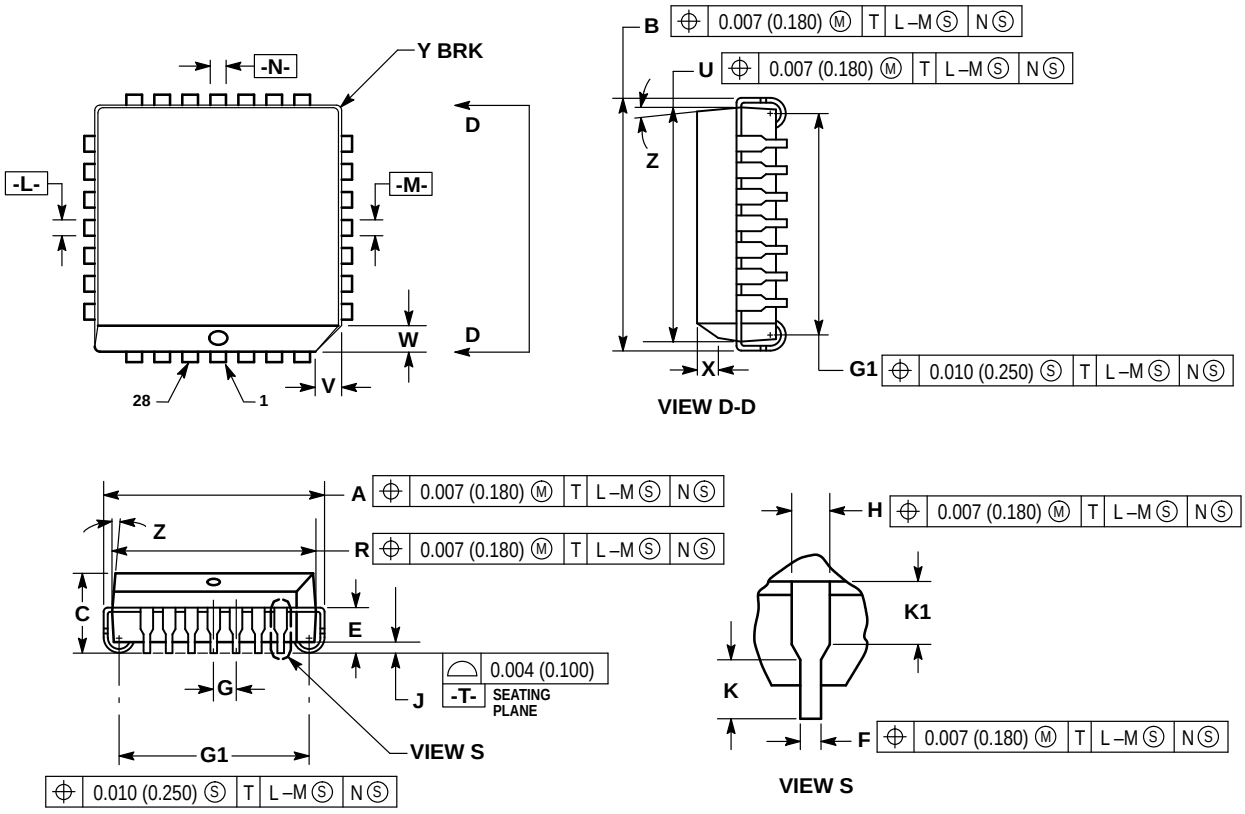

NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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