M65821FP
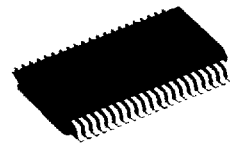
CD PLAYER DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The M65821FP is a signal processing LSI using silicon gate CMOS technology for use in a compact disc (CD) player. The M65821FP incorporates the functions of data slicer, PLL for clock extraction from HF data, demodulator, decoder, error corrector, interpolator, 4fs digital filter, digital interface and disc motor speed control in single chip.

FEATURES

- Adjustment free EFM-PLL (VCO built-in) with a wide lock range
- Jitter margin ± 8 frame
- Easy-to-handle CLV servo command
- Sufficient mute control (zero-cross/fade mute)
- Lch/Rch monaural output
- Attenuation can be designated independently for L & R channels
- Error flag output in one byte
- High-performance 4-Fs digital filter
- 18-bit/20-bit outputs available
- Centralized control by microcomputer serial command
- Lower power dissipation during standby in the sleep mode
- Digital de-emphasis circuit built-in
- Digital silent detector circuit built-in
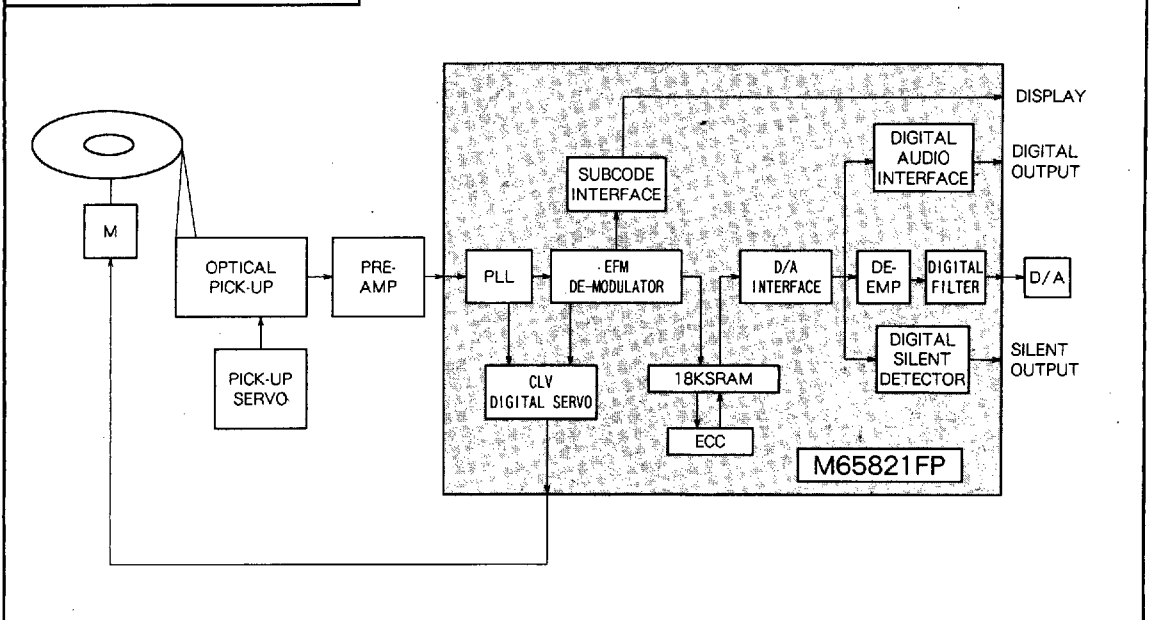- Reduced base area by a smaller package

Outline 42P2R-A

0.8mm pitch 450mil SSOP
(8.4mm × 17.5mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ··························· V_{DD} = 4.5 to 5.5V
Rated supply voltage ····························· V_{DD} = 5V
Rated power dissipation ························· 125mW

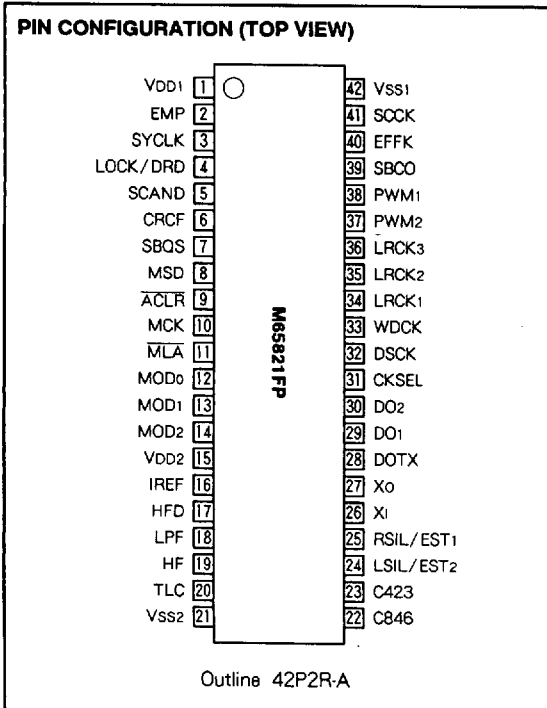## SYSTEM BLOCK DIAGRAM

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M65821FP

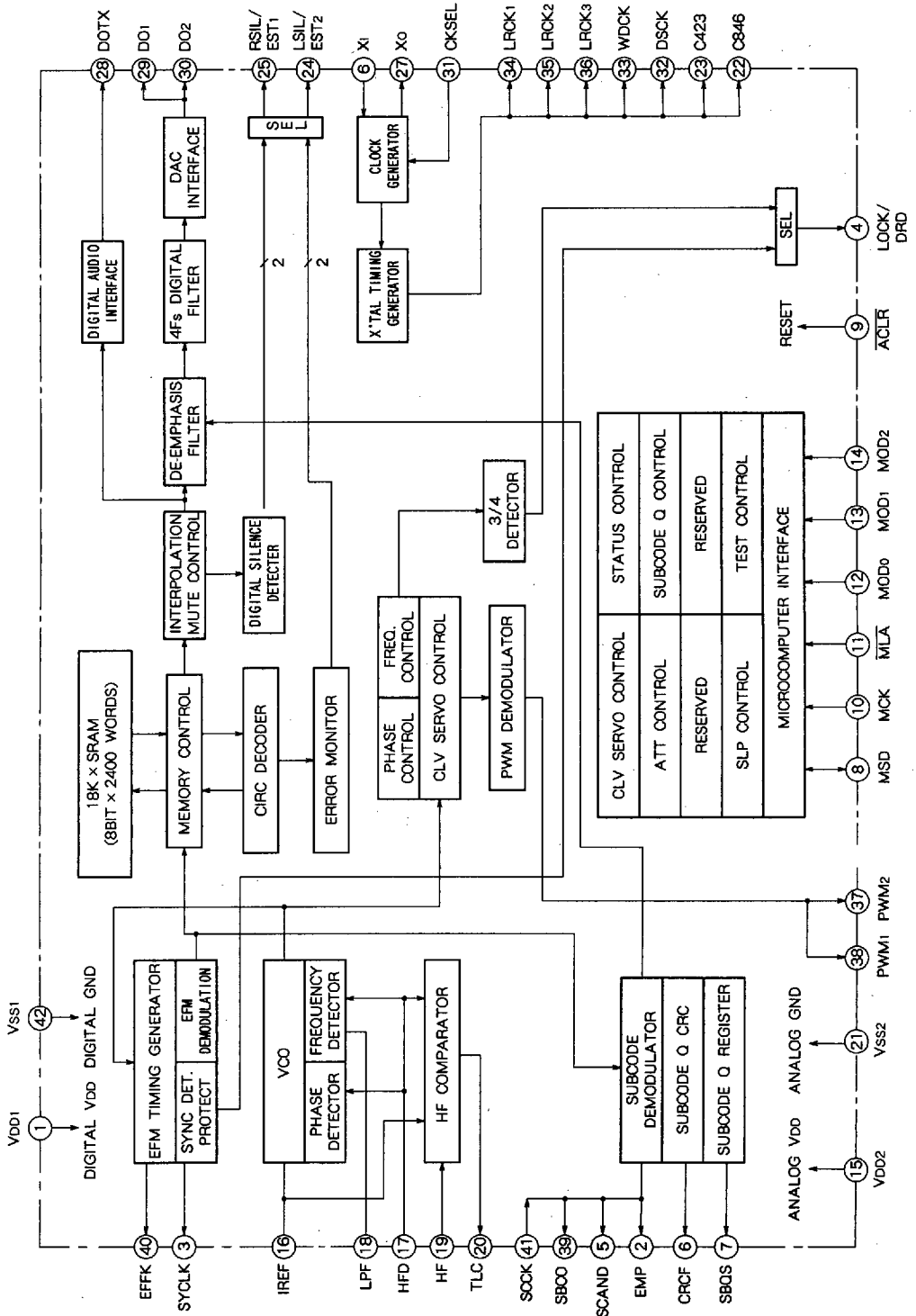## CD PLAYER DIGITAL SIGNAL PROCESSOR

BUILT-IN FUNCTIONS

● Adjustment free EFM-PLL
· Slice level control
· Bit clock generation
· Adjustment free VCO
● Demodulation & Decoding
· EFM demodulation
· Frame sync detection, Protection & interpolation
· Subcode demodulation (serial)
· Subcode Q-CRC check
· Subcode Q register
· Emphasis detection
· Jitter absorption ± 8 frame
· CIRC decoding
    Unscrambling
    De-interleaving
    Error-correction capability C1 : Duplex ; C2 : Duplex
· Interpolation processing (average value Interpolation & previous value hold)
· Error monitor output
· Interpolation inhibit
· Zero cross mute
· Fade mute
· Digital attenuator
· Dual DAC output
· L/R monaural output

● Digital filter
· 4 times oversampling phase linear digital filter
· Digital filter-thru
· 18-bit/20-bit output (only when a digital filter is used)
● CLV digital servo
· Low disk rotation detection
· PWM output
● Digital de-emphasis
· Automatic detection of emphasis flag
· Intermnal/external emphasis changeover
● Digital silence detector
· Audio data silence detection
● Microcomputer interface
· Mute, attenuation, disk motor ON/OFF, disk motor brake control
   · Digital-OUT ON/OFF, fade mute selection, digital filter through selection, interpolation inhibit selection, clock precision input, 18-bit output selection, 20-bit output selection, dual DAC selection, stereo/monaural selection
· Attenuation level control
· Subcode Q register interface
· Sleep mode control
● Digital audio interface
· Digital-OUT ON/OFF
· Clock precision input
● Master clock changeover
· Master clock 8.4672MHz/16.9344MHz selectable

PIN CONFIGURATION (TOP VIEW)

Pin	Signal		Pin	Signal
1	VDD1		42	VSS1
2	EMP		41	SCCK
3	SYCLK		40	EFFK
4	LOCK/DRD		39	SBCO
5	SCAND		38	PWM1
6	CRCF		37	PWM2
7	SBQS		36	LRCK3
8	MSD		35	LRCK2
9	$\overline{ACLR}$		34	LRCK1
10	MCK		33	WDCK
11	$\overline{MLA}$		32	DSCK
12	MOD0		31	CKSEL
13	MOD1		30	DO2
14	MOD2		29	DO1
15	VDD2		28	DOTX
16	IREF		27	Xo
17	HFD		26	XI
18	LPF		25	RSIL/EST1
19	HF		24	LSIL/EST2
20	TLC		23	C423
21	VSS2		22	C846

M65821FP

Outline 42P2R-A

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CD PLAYER DIGITAL SIGNAL PROCESSOR

BLOCK DIAGRAM

PIN DESCRIPTION

Pin No.	Name	I/O	Function
①	V_{DD1}	–	Digital system V_{DD}
②	EMP	O	Emphasis output. : "H" for emphasis
③	SYCLK	O	Frame lock status output. Lock = H
④	LOCK/ DRD	O	Sync status & low disk rotation staus output
⑤	SCAND	O	Subcode sync signal output : "H" for sync
⑥	CRCF	O	CRC checked results of subcode Q : CRC OK = H
⑦	SBQS	O	subcode Q register read interrupt signal. : "L" for read-around
⑧	MSD	I/O	Microcomputer interface serial data I/O
⑨	ALCR	I	System reset input : reset = L
⑩	MCK	I	Microcomputer interface shift clock
⑪	MLA	I	Microcomputer interface latch clock
⑫	MOD_0	I	Microcomputer interface mode 0
⑬	MOD_1	I	Microcomputer interface mode 1
⑭	MOD_2	I	Microcomputer interface mode 2
⑮	V_{DD2}	–	PLL system V_{DD}
⑯	IREF	I	PLL circuit reference current setting
⑰	HFD	I	High frequency signal missing detect input
⑱	LPF	I/O	PLL loop filter
⑲	HF	I	High frequency signal input
⑳	TLC	O	Slice level control output
㉑	V_{SS2}	–	PLL system V_{SS}
㉒	C846	O	Crystal system 8.4672MHz clock output
㉓	C423	O	Crystal system 4.2336MHz clock output

Pin No.	Name	I/O	Function
㉔	LSIL/ EST_2	O	Lch silence data output : error status output 2 : "H" at C_2 decoder error detection
㉕	RSIL/ EST_1	O	Rch silence data output : error status output 1 : "H" at C_1 decoder error detection
㉖	X_I	I	Crystal oscillator input : feedback resistor built in
㉗	X_O	O	Crystal oscillator output
㉘	DOTX	O	Digital-OUT output
㉙	DO_1	O	Audio serial data output for DAC : Lch output at dual DAC mode
㉚	DO_2	O	Rch output at dual DAC mode : LRCK1 inversion at single DAC mode
㉛	CKSEL	I	Master clock selection input (H : 8MHz, L : 16MHz)
㉜	DSCK	O	Data shift clock for DAC
㉝	WDCK	O	Word clock for DAC
㉞	$LRCK_1$	O	LR clock 1 for DAC
㉟	$LRCK_2$	O	LR clock 2 for DAC
㊱	$LRCK_3$	O	LR clock 3 for DAC
㊲	PWM_2	O	Disc motor drive PWM output 2 (acceleration side)
㊳	PWM_1	O	Disc motor drive PWM output 1 (deceleration side)
㊴	SBCO	O	Subcode serial output
㊵	EFFK	O	EFM frame clock output. duty ≒ 50%
㊶	SCCK	I	Shift clock input for serial subcode data output
㊷	VSS_1	–	Digital system V_{SS}

CD PLAYER DIGITAL SIGNAL PROCESSOR

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Rating	Unit
V_{DD}-V_{SS}	Supply voltage	− 0.3 to + 7	V
V_I	Input voltage	V_{SS}-0.3≤V_I≤V_{DD}+0.3	V
V_O	Output voltage	V_{SS} ≤ V_O ≤ V_{DD}	V
P_d	Power dissipation	350	mW
T_{opr}	Operating temperature	−10 to +70	℃
T_{stg}	Storage temperature	−40 to +125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	Input voltage ("H" level)		0.7V_{DD}	−	V_{DD}	V
V_{IL}	Input voltage ("L" level)		V_{SS}	−	0.3V_{DD}	V
f_{osc}	Oscillation frequency (X'tal)	Normal speed		8.4672		MHz
		Double speed		16.9344		MHz
f_{vco}	Oscillation frequency (VCO)	Normal speed		8.6436		MHz
		Double speed		17.2872		MHz

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{DD} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	Ta = − 10~ + 70℃	4.5	5.0	5.5	V
I_{DD}	Circuit current	f_{osc} = 8.4672MHz f_{vco} = 8.6436MHz	−	46	70	mA
V_{OH}	Output voltage ("H" level)	V_{DD}=4.5V, I_{OH}=−0.8mA	3.5	−	−	V
V_{OL}	Output voltage ("L" level)	V_{DD}=4.5V, I_{OL}=0.8mA	−	−	0.4	V
I_{IH}	Input current ("H" level)	V_{IH}=4.5V	−	−	2	μA
I_{IL}	Input current ("L" level)	V_{IL}=0.5V	−	−	− 2	μA
I_{OZH}	Output current in OFF-state ("H" level)	V_{OH}=4.5V	−	−	2	μA
I_{OZL}	Output current in OFF-state ("L" level)	V_{OL}=0.5V	−	−	− 2	μA
f_{vco1}	VCO(EFFK)	V_{LPF}=1.0V	−	−	2.0	kHz
f_{vco2}	free-running frequency	V_{LPF}=2.5V	−	7.2	−	kHz
f_{vco3}	(R_{IREF} = 180kΩ)	V_{LPF}=4.0V	12.0	−	−	kHz
V_{T-}	Schmitt trigger * input voltage		1.5	2.0	2.5	V
V_{T+}			2.0	2.5	3.0	V
V_H			0.1	0.5	1.5	V
R_{pu}	Pull up resister		10	20	40	kΩ

CHARACTERISTICS OF SCHMITT TRIGGER
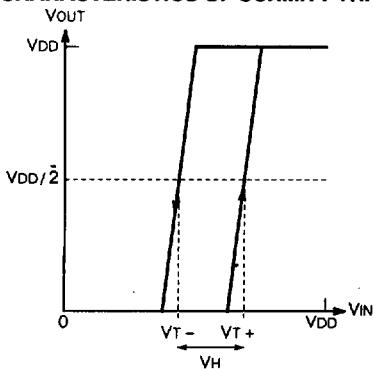
* Applied pin : ALCR, MCK, MLA, MOD0, MOD1, MOD2, CKSEL, SCCK

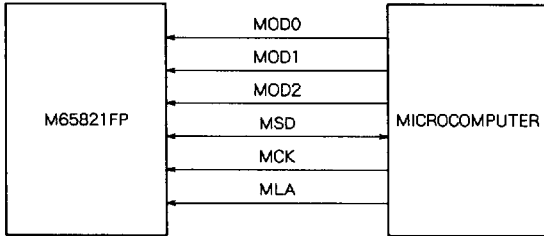Applied pin of pull up resister : MCK, MLA, MOD0, MOD1, MOD2, CKSEL, SCCK

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FUNCTION DESCRIPTION

1. MICROCOMPUTER INTERFACE

(1) Connection

Pin No.	Signal name	Contents	I/O
⑫ to ⑭	MOD0 to MOD2	Mode selector pin	I
⑧	MSD	Microcomputer serial data I/O pin	I/O
⑩	MCK	Microcomputer serial clock input pin	I
⑨	MLA	Microcomputer data latch signal input pin	I

(2) Explanation of modes

Mode	Mode selector pin			Data contents	I/O	Number of bytes
	MOD2	MOD1	MOD0			
0	L	L	L	CLV servo control	I	1
1	L	L	H	Status control	I	2
2	L	H	L	Attenuate register control	I	2
3	L	H	H	Subcode Q register control	O	10
4	H	L	L	RESERVED	–	–
5	H	L	H	RESERVED	–	–
6	H	H	L	Sleep mode	I	0
7	H	H	H	Test mode (for delivery sorting)	I	0

Note : I/O is as viewed from M65821FP

(3) Microcomputer I/O timing

Input timing (M65821FP ⇐ Microcomputer)   Output timing (M65821FP ⇒ Microcomputer)
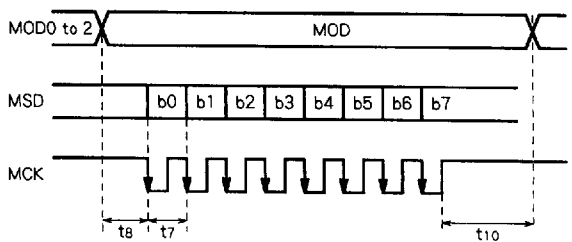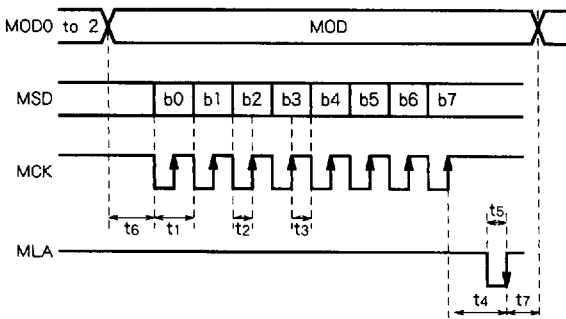
Symbol	Description	Min	Unit
t_1	Shift clock width	200	nsec
t_2	Shift clock setup time	100	nsec
t_3	Shift clock hold time	100	nsec
t_4	Latch clock setup time	200	nsec
t_5	Latch clock width	200	nsec
t_6	Mode setup time	250	nsec
t_7	Mode hold time	200	nsec

Symbol	Description	Min	Unit
t_7	Shift clock width	200	nsec
t_8	Mode setup time	250	nsec
t_{10}	Mode hold time	200	nsec

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CHARACTERISTICS OF SLEW RATE

Applied pin : MCK, SCCK
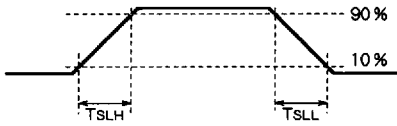
Symbol	Condition	Min	Typ	Max	Unit
T_{SLH}	$4.5V \leqq V_{DD} \leqq 5.5V$	–	–	1.0	msec
T_{SLL}		–	–	1.0	msec

(4) Mode 0:CLV servo control [Mode 0 : MOD2 to 0 = (0, 0, 0)]

CLV servo, mute, attenuate and fade mute are contriolled by cotrolling the register in mode 0.

Register name	Function		Register contents							
			b0	b1	b2	b3	b4	b5	b6	b7
DUMMY	Don't care		X							
S/S	Disc motor start/ stop control	Stop		0						
		Start		1						
BCON	Control for disc motor braking	Braking			0					
		No braking			1					
BRAK	Disc motor brake control	Brake OFF				0				
		Brake ON				1				
ATT	−12dB attenuation control	ATT OFF					0			
		ATT ON					1			
MUTE	Mute control	MUTE ON						0		
		MUTE OFF						1		
S/S timer reset	S/S timer (0.3s) reset control	Timer operation							0	
		Timer reset							1	
IC code	Identification signal	Servo								0
		DSP								1
Initial state	Register contents in reset conditions		0	0	0	1	0	0	1	0

(5) Mode 1:Status control [Mode 1 : MOD2, 1, 0 = (0, 0, 1)]

By setting a register in mode 1, it is possible to determine the status required in operating the signal processing unit.

The status register consists of 2 bytes, and setting is possible by starting up MLA after inputting 2-byte data to DSP.

[1 byte]

Register name	Function		Register contents							
			b0	b1	b2	b3	b4	b5	b6	b7
DOUT	Control for use digital-OUT	Used	0							
		Not used	1							
NON-AUDIO	Control for audio or non-audio data	Audio		0						
		Non audio		1						
DFPASS	Controls for digital filter	Used			0					
		Pass			1					
18-BIT	Control for 18-bit output	16-bit output				0				
		18-bit output				1				
20-BIT	Control for 20-bit output	16-bit output data					0			
		20-bit output					1			
DUAL-DAC	Control for single or dual DAC mode	SINGLE						0		
		DUAL						1		
LMONO	Lch monaural output	Stereo							0	
		L-ch monaural							1	
RMONO	Rch monaural output	Stereo								0
		R-ch monaural								1
Initial state	Register contents in reset conditions		0	0	0	0	0	0	0	0

[2 byte]

Register name	Function		Register contents							
			b0	b1	b2	b3	b4	b5	b6	b7
FMUTE	Controlling fade mute ON/ OFF (See Note)	Fade-out	0							
		Fade-in	1							
FMTC	Controlling the fade mute time	2.2sec		0						
		34.8ms		1						
FMCNT	Fade mute used/not used	Not used			0					
		Used			1					
ZMCM	Controlling zerocross mute or no zerocross mute	Zerocross present				0				
		No Zerocross				1				
ACCK	Oscillation precision input	Level II					0			
		Level III					1			
DDEC	Controlling the presence or absence of digiral de-emphasis	Internal emphasis						0		
		External emphasis						1		
SIL/EST	Controlling silence output and error monitor output	Silence output							0	
		Error monitor output							1	
SILC	Controlling silence output	Stereo								0
		Monaural								1
Initial state	Registers contents in reset conditions		0	0	0	0	0	0	0	0

Note 1. The FMUTE register changing point is detected for operation
· Fade in when "0" changes to "1"
· Fade out when "1" changes to "0"
2. When the FMCNT register is "1", the attenuate register becomes effective.
3. The status data input sequence is as follows
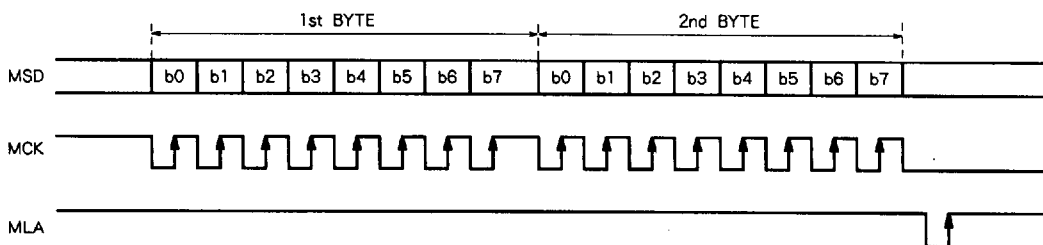
(6) Attenuate register control [Mode 2 : MOD2, 1, 0 = (0, 1, 0)]

The attenuation level can be set independently for L and R channels by using the attenuate register.

This register is set, using 8-bit for L and R channels : this setting is carried out by inputting a clock to the MSD pin with LSB first. from L-channel side.

MSD, MCK, and MLA at this time are shown below :
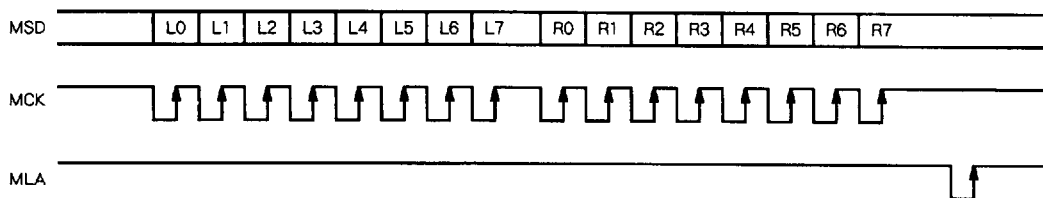
The relation between the attenuation data and attenuation level is shown in para. 10.(4).

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(7) Subcode Q register interface [Mode 3 : MOD2, 1, 0 = (0, 1, 1)]

The data of subcode Q stored in the internal 80-bit register can be read with a serial clock from the microcomputer.

When MOD2, 1, 0 = (0, 1, 1), MSD is placed in output conditions, and the register is set by inputting 80 clocks to the MCK pin from SBQS pin rise to the next SBQS fall. The data from the MSD pin is output with MSB & LSB inverted in 8-bit.

The SBQS pin outputs "L" when the following conditions are satisfied and the internal register is placed in readable conditions.

< Conditions under which the SBQS pin is placed in "L" >
(a) When the CRC checked results is OK
(b) When both subcode sync signals S_0, S_1 are detected in the specified position. (S_0 and S_1)
When both conditions (a), (b) above are satisfied, the SBQS pin outputs "L".
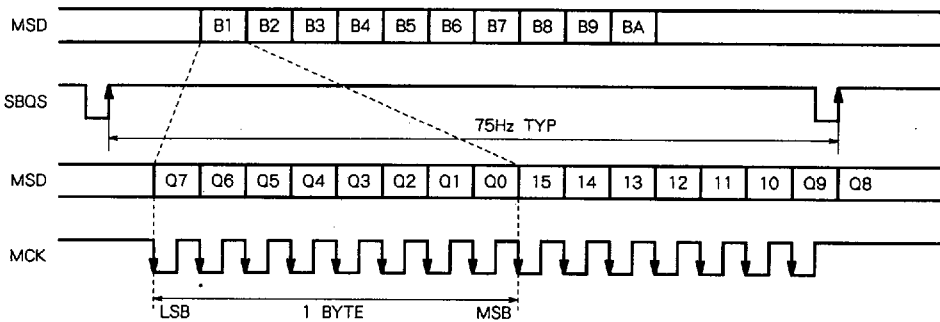
The emphasis information of subcode Q data is output to the EMP pin.

Condition	EMP pin
When no emphasis is present	L
When emphasis is present	H

(8) Sleep mode   [Mode 6 : MOD2, 1, 0 = (1, 1, 0)]

The sleep mode is used when LSI is not used : the master clock stops, and the low power dissipation mode is selected. The sleep mode is selected by inputting "L" to the MLA pin when MOD2, 1, 0 = (1, 1, 0). To release to the sleep mode, set the ALCR pin to "L" once and set it to "H" again.
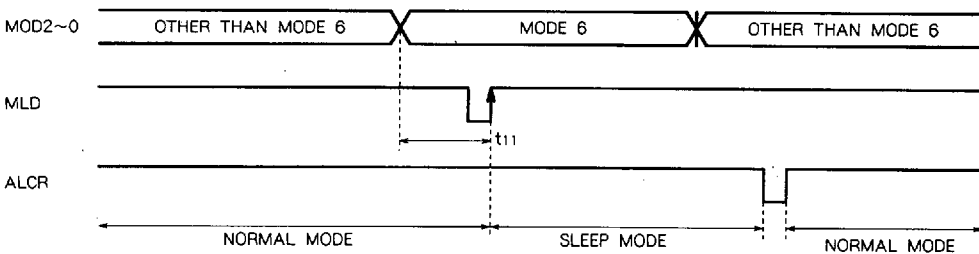
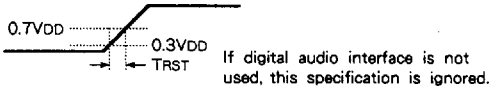| Symbol	Description	Min	Unit
t_{11}	Set-up time of mode 6 latch signal	250	nsec

(9) Test mode   [Mode 7 : MOD2, 1, 0 = (1, 1, 1)]

This mode is used when LSIs are tested before shipment : it is a use inhibit mode.

Mode 7 is set by latching with the MLA signal in the same matter as in mode 6 ; even when MOD2 to 0 is (1, 1, 1) momemtarily when the mode is switched, it is not latched to the inside.

CD PLAYER DIGITAL SIGNAL PROCESSOR

(10) Reset input timing (Only digital audio interface mode)

0.7VDD ⋯⋯⋯⋯

0.3VDD

→| |← TRST

If digital audio interface is not used, this specification is ignored.

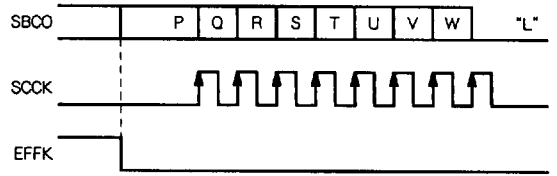| Symbol	Condition	Min	Typ	Max	Unit
TRST		–	–	10.0	msec

2. SUBCODE INTERFACE

The subcode data (P, Q, R, S, T, U, V, W), can be read from the SBCO pin by inputting a clock to the SCCK pin among the data coverted from 14-bit EFM signal to 8-bit symbol. When both subcod sync patterns S_0, S_1 are detected in the specified position as a sync signal of this subcode, a sync signal is output from the SCAND pin.

If 8 clock or more are input to the SCCK, the SBCO is placed in "L".

SBCO ... | P | Q | R | S | T | U | V | W | "L"

SCCK

EFFK

3. EFM-PLL CIRCUIT

(1) Data slicing/PLL

The M65821FP has an analog front-end for incoming HF (EFM) signal. Using CMOS-Analog technology, the front-end comprises an automatic slice level control circuit and EFM-PLL circuit with internal adjust-free VCO. The block-diagram shows the analog front-end. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through the external CR. If HFD goes High because of a defect an disc, then TLC time off and holds the DC level.

EFM-PLL extracts the EFM clock signal from the HF signal. The PLL circuit has a phase/frequency detector providing the M65821FP with a wide capture/lock range. There is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO. LPF froms off if HFD goes High.

IREF is the reference current input used to determine the current of charge pumps of TLC and LPF, operating point of HF comparator and VCO free running frequency. If IREF is connected to a noisy power supply through a resistor, VCO is modulated and the error-rate increases. Therefore, power supply noise at IREF must be held to a minimum.
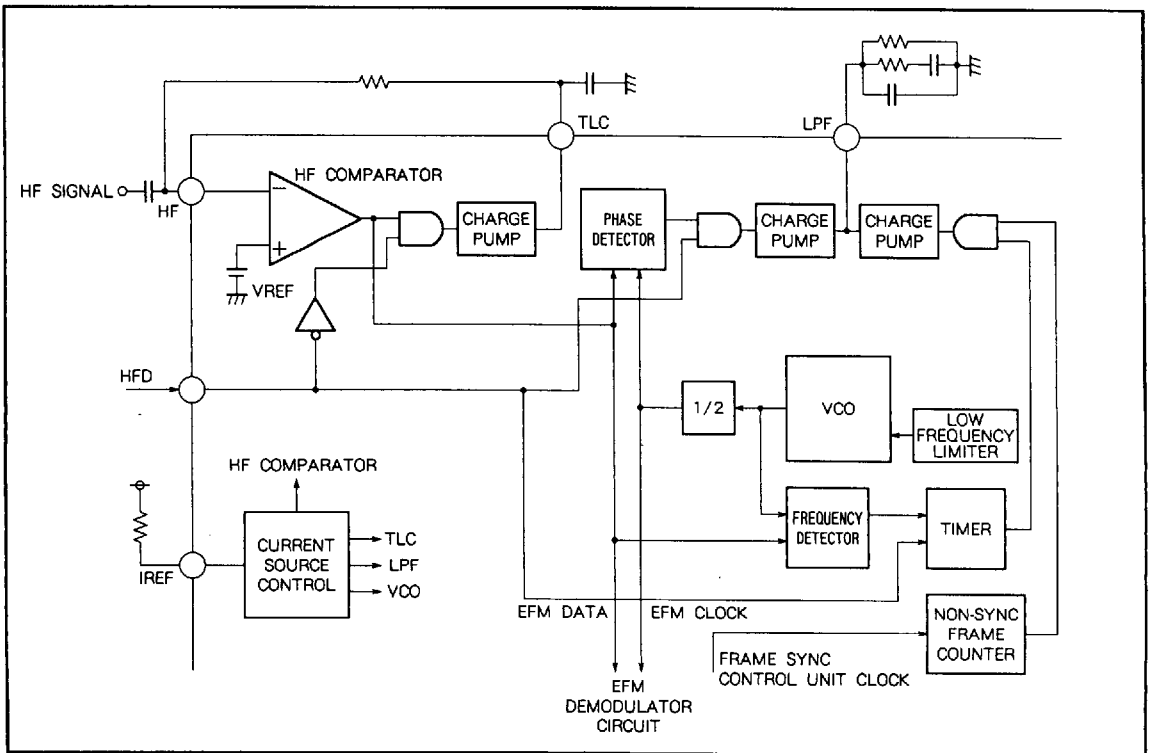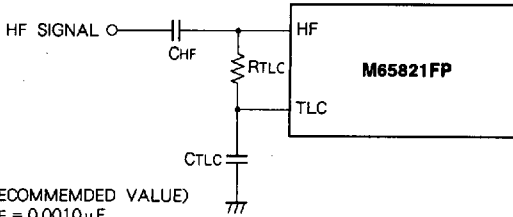

Fig. 1 Block diagram of the analog front end
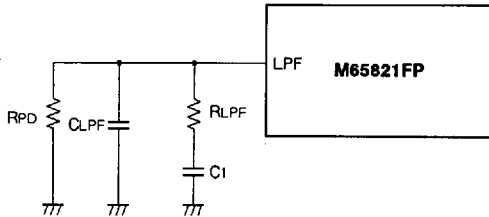
(2) Slice level control

(RECOMMEMDED VALUE)
$C_{HF} = 0.0010 \mu F$
$C_{TLC} = 0.022 \mu F$
$R_{TLC} = 33k \Omega$
Vin HF 0.5VP–P Min

A slice level control circuit is formed by connecting a resistor and capacitors to the HF (High-frequency signal input) pin and TLC (Slice level control output) pin.

(3) PLL circuit

(RECOMMENDED VALUE)
$C_{LPF} = 470pF$
$C_1 = 0.15 \mu F$ to $1.0 \mu F$
$R_1 = 2.2k \Omega$
$R_{PD} = 3.3M\Omega$

Since the adjustment-free VCO is built in, the adjustment-free PLL circuit can be formed by connecting a resistor and capacitors to the LPF (Low-pass filter) pin.
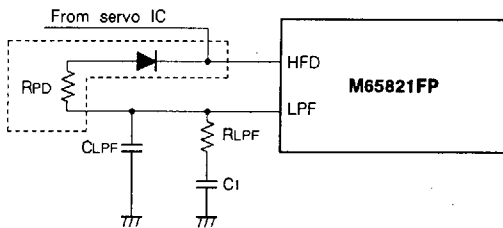
(RECOMMENDED VALUE)
$C_{LPF} = 470pF$
$C_1 = 0.15 \mu F$ to $1.0 \mu F$*
$R_{LPF} = 2.2k \Omega$
$R_{PD} = 3.3M\Omega$

The error rate characteristics of defect disc is imploved by connecting R_{PD} to HFD using dioade.
From $0.15 \mu F$ to $1.0 \mu F$ capacitor is available for C_1.
In high speed search such as track count search, the rotation of disc decrease. If this is problem, this problem is improved by using large C_1. (See sec. 5 –(3))

(4) Reference current setting
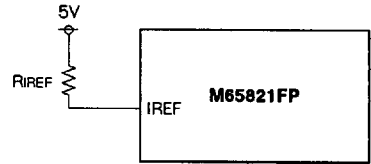
(RECOMMENDED VALUE)
$R_{IREF} = 180k\Omega$ (Normal speed)
$R_{IREF} = 150k\Omega$ (Double speed)

A resistor must be connected between the IREF pin and V_{DD} in order to set the reference current used in determining the current values of the TLC pin and LPF pin, the compatator operating current of the slice level control circuit, and the VCO free-run frequency.

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4. EFM DEMODULATOR

EFM signal converted to the logic level and clock reproduced from EFM signal are input to the demodulator block, which is then converted to an 8-bit symbol data.

This EFM signal demodulation is based on the EFM conversion table specified in the RED book.

To demodulate EFM signal, the demodulator circuit should be synchronized in frames for EFM signal.

The sync circuit has a system of protecting sync even when a sync pulse is missing and preventing sync errors in bit slip or re-pull-in from pull-out, thus maintaining stable sync even for disc defects (flaws & stains).

The block diagram for this frame sync control is shown in Fig. 2 below.
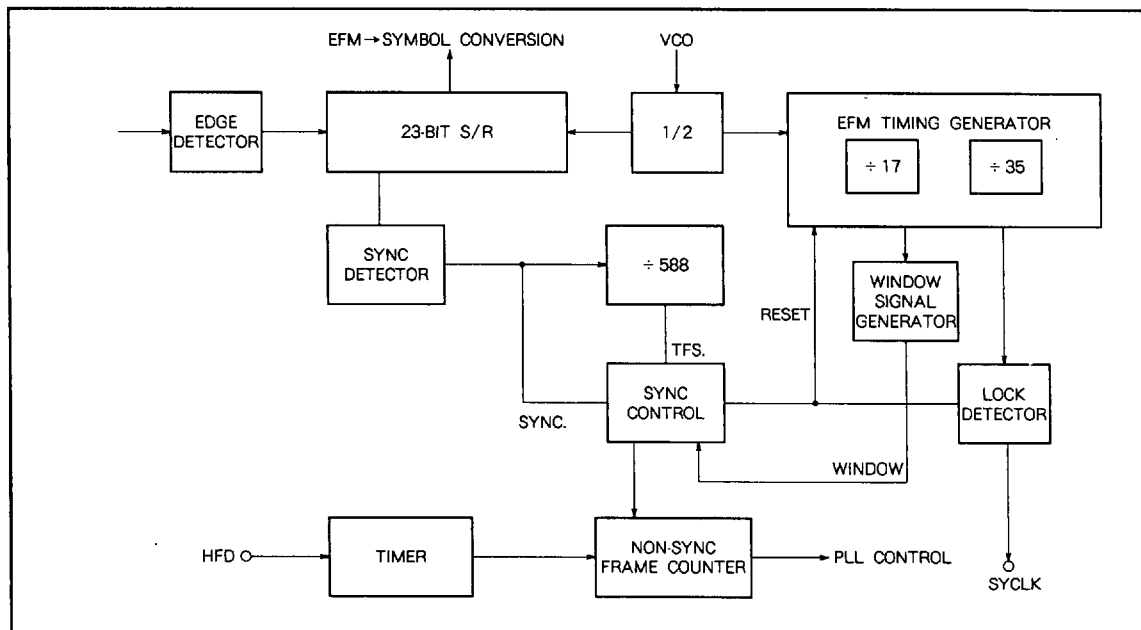

Fig. 2 Frame sync control unit block diagram

In the block diagram above, the conditions of generating counter reset signal, "Reset" in the EFM timing generation unit can be expressed in the following equation.

$$\text{Reset} = \text{Sync} * \text{Tfs} + \text{Sync} * \text{Window}$$

(where : $*$ = Logical product AND $+$ = Logical sum OR)

In this equation, Sync, Tfs and Window mean a sync signal, a detection signal of sync signal spacing ($= 588$), and $\pm 7C$ window signal respectively.

In the synchronizing conditions, Sync and Tfs generate at the same time, and Sync enters the window center. In this state, it follows that "H" is output to SYNCLK pin and EFM signal is synchronizing in frames.

Contents	SYCLK
EFM signal is not in synchronizing in frames	L
EFM signal is synchronizing in frames	H

To monitor a synchronous condition with a control microcomputer, it is necessary to provide a signel from which a short-period missing of sync pattern due to a disc defect, which occurs even in a synchronizing state is eliminated.

In M65822AFP, this signal is allocated to LOCK/DRD pins. When the braking instruction from the microcomputer is not input, the LOCK/DRD pins monitor the synchronizing state in 1/16period of EFM frame clock, outputting the results. If the monitored results are sync, "H" is output, and if they are not sync continuosly 8 times, "L" is output.(When the braking instruction is input from the microcomputer, the LOCK/DRD terminals output a low disc rotation status monitor signal (DRD signal). The details are described later in the CLV servo control paragraph.)

Conditions	Contents	LOCL/DRD
Not in a braking condition	EFM signal is not synchronizing in 1/16 frames	L
	EFM signal is synchronizing in 1/16 frames	H
Braking condition	Low disc rotation status monitor signal 8/DRD signal	DRD signal

5. CLV SERVO CONTROL

(1) PWM control

The CLV servo control circuit controls the disc motor with the frequency difference between the clock reproduced from EFM signal and clock obtained from the standard oscillator, and the address difference in internal RAM writing.

The motor control output is transmitted to PWM1 (deceleration output) and PWM2 (acceleration output) pins in PWM waveform.

Since the phase is internally compensated. the CLV servo circuit can be configured by just connecting a driver to the PWM1 and PWM2 pins outputs.

Fig. 3, shows the CLV waveform and its duty.

In the CIRC composite section, the duty is reset to 0 where the address difference between built-in RAM wrtie and read exceeds ±8 frames.

In this figure, the point in which the waveform width of acceleration output and deceleration output is equal is shown as dut "0".

The disc motor can be driven even when the PWM waveform is used directly or even through and analog signal in which PWM1 & PWM2 outputs are integrated.

When the disc motor is driven with an analog signal, servo gain can be set externally.

When it is driven with a PWM waveform, however, the PWM waveform cannot adjust the duty from the outside; therefore, the servo chracteristics are determined with the motor torque or disc turntable, disc retaining angular moment, etc.

Pin / Mode	KICK	CLV	BRAKE	OFF
PWM2 (Acceleration)	H	*	L	L
PWM1 (Deceleration)	L	*	H	L

$$DUTY = \frac{W_{PWM2} - W_{PWM1}}{W_{PWM2} + W_{PWM1}}$$

Fig. 3 CLV waveform

(2) Low disc rotation control

When playback is suspended, disc rotation should be stopped securely. The LOCK/DRD pin monitors the PLL oscillation frequency the disc is being braked with an instruction from the microcomputer, and outputs "H" if it detects a frequency lower than 3/4 of that in normal playback.

By adjusting the period of a brake signal with this signlal, disc rotation can be stopped.
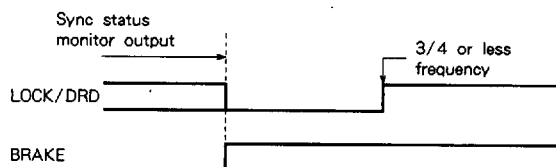
Conditions	Contents	LOCL/DRD
Not in a braking state	Sync status monitor output	LOCK
Braking state	The PLL oscillation frequency is more than 3/4 of that in normal playback	L
	The PLL oscillation frequency is less than 3/4 of that in normal playback	H

(3) High speed search

In case of high speed search such as track count search, the disc rotation may unstable in search mode.

Because the false lock protection circuit is working in search mode by long time unlock. The false lock protection circuit can stop to work by using BRAK register in MOD0.
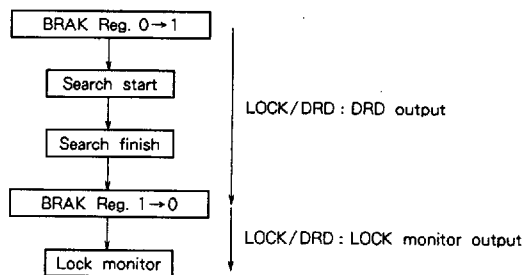
When BRAK register is 1, the false lock protection circuit stop to work and the disc rotation can improve in search mode. When BCON register is 1 S/S register is 0 and BRAK register is 1, brake function is working. If BCON register is 0 or S/S register is 1, brake function is not working. But when BRAK register is 1, LOCK/DRD output DRD signal. So it is necessary to change BRAK register from 1 to 0, when search is completed.

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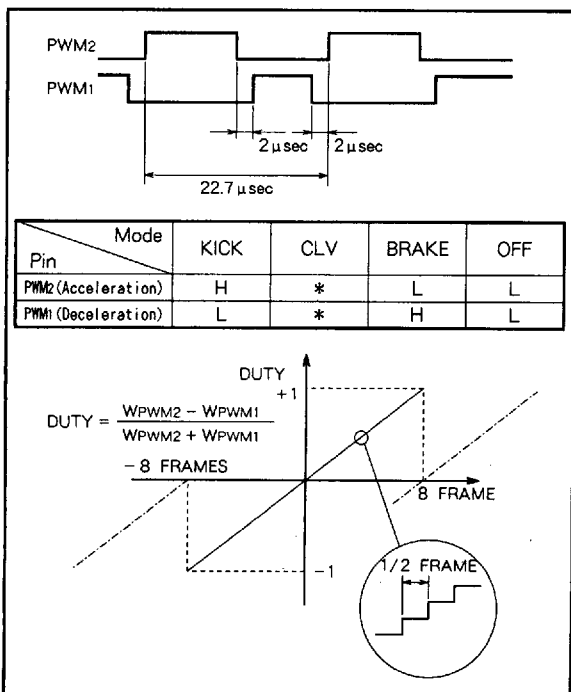
6. ERROR CORRECTION

(1) Correction ability

Both decoders C1, C2 correct dual errors Max.

(2) Error monitor output

The error status detected at decoding is output to pins EST_1, EST_2.

If an error is detected with decoder C1, "H" is output to pin EST_1 for its frame. and "H" is output to pin EST_2 for an erroneous word judged to be uncorrectable with decoder C2.

If a non-audio data is selected in mode 1 of microcomputer, interface, no output data is interpolated,and the error status of decorder C2 is output to the data (each byte) detected as uncorrectable.

If an audio data is selected, the error status is output to the interpolated word (2 bytes).

For detailed timing, refer to "D/A Interface"
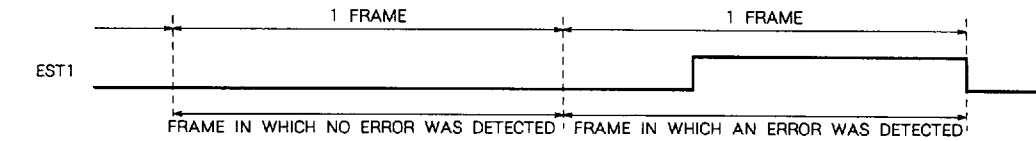
(a) For audio data
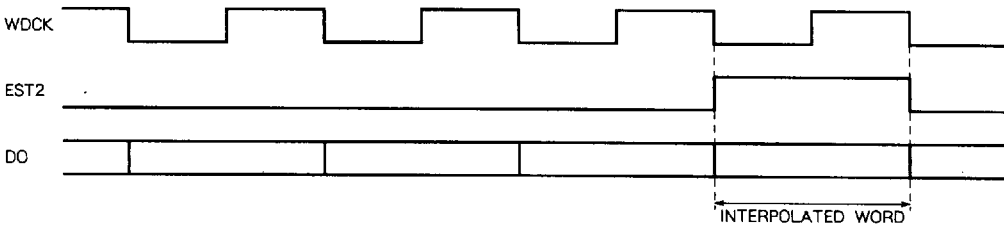
(b) For non-audio data
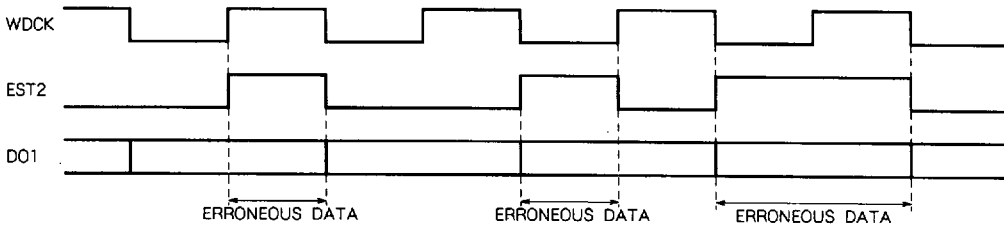
(3) Interpolation

The average value is interpolated or the porevious value hold is interpolated for the word that cannot be corrected by decoder C2, thus preventing noise from generating.

If the anterior and posterior words from which an error was detected prove correct after detection, the average value interpolation is carried out, and in other cases, the previous value hold is carried out.

However, if the non-audio data is selected in mode 1, no interpolation processing is performed . (Refer to "MICROCOMPUTER INTERFACE".)
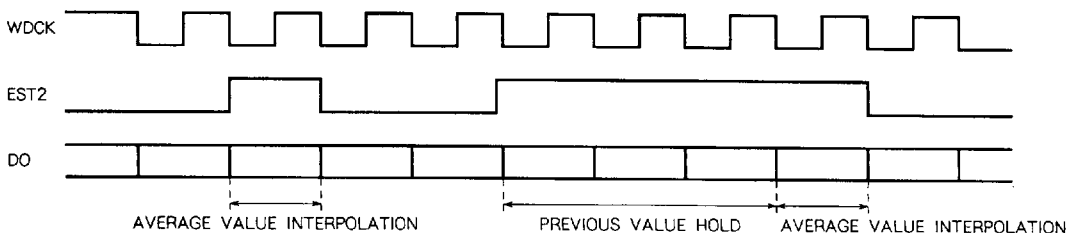
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7. DIGITAL OUT

The digital audio signal formatted according to EIAJ Standard CP-340 "Digital Audio Interface" is outputted to DOTX pin.

The validity flag is internally set to "1" automatically when the interpolated word is transmitted.

The user data, which is read in the subcode interface circuit, is transmitted. Channel clock precision can be set from the outside so that it is compatible with the validity pitch.

The channel status is set to level III in the validity pitch, mode, and level II is set autometically when it is not in the validity pitch mode.

of mode 1 of microcomputer interface.

B : CHANNEL L AND TOP OF BLOCK
M : CHANNEL L EXCEPT TOP OF BLOCK
W : CHANNEL R

PARITY BIT
CHANNEL STATUS
USER DATA
VALIDITY FLAG

SYNC	AUX	EXTENDED BIT	AUDIO DATA	V	U	C	P
4 BIT	4 BIT	4 BIT	LSB 16 BIT MSB	1	1	1	1

Sub frame format

M	L CHANNEL	W	R CHANNEL	B	L CHANNEL	W	R CHANNEL	M	L CHANNEL

FRAME 191   FRAME 0   FRAME 1
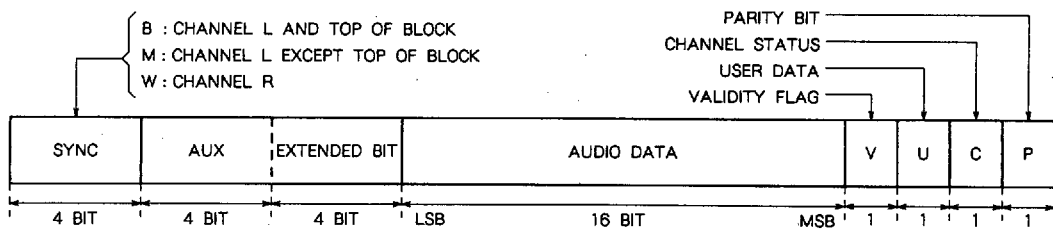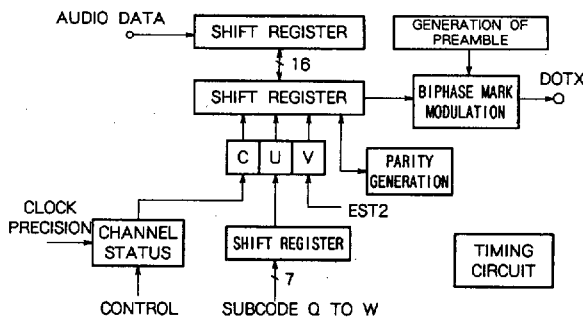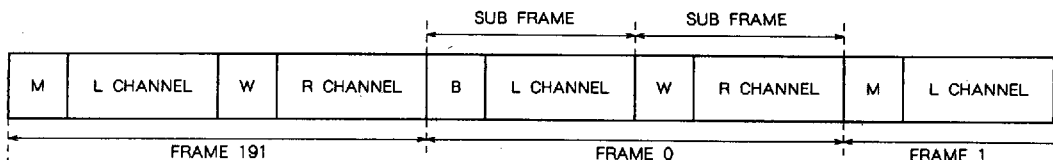
Frame format
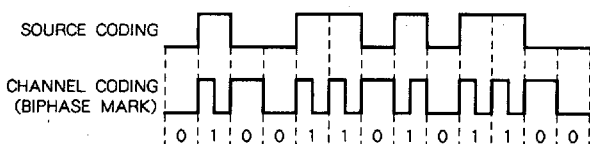
Channel coding (Biphase mark modulation)

When the Dout register is "H", the digital interface output is stopped to prevent from radiation.

Chanel status is set as follows.

ID1, COPY and EMP data in subcode Q data transfer to the channel status register in digital audio interface, when CRC is OK and subcode synchronization pattern S0 and S1 are detected in right position.

EST2 flag copy to validity flag.

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8. THE DIGITAL FILTER

The data of sampling frequency 44.1kHz is converted to that of sampling frequency 176.4kHz at 4 times over-sampling by FIR phase linear digital filter. It is also possible to output deta of 18-bit and 20-bit that were computed by the digital filter. The digital filter may also pass according to the purposes : a high-precision digital filter is connected externally, and this filter is suitable for signal processing that handles non-audio data, such as CD-ROM as well.

The characteristics in over-sampling are shown in Fig. 4 below.

9. DIGITAL DE-EMPHASIS

M65822AFP has a built-in digital de-emphsis circuit containing a primary IIR filter. When DDEC bit of the status register is in "L", the source emphasis information is detected : if emphasis is rresent, the de-emphasis ciruit of 50 /15(μ) operates automatically.

When DDEC bit is in "H", the intermal de-emphsis circuit is disabled regardless of presence or absence of emphasis information, and only emphasis information is output from EMP pin. (When DDEC bit is in "L", emphasis information is also output from EMP pin.)

The following is the chracteristic chart for the de-emphsis circuit built in the M65822AFP.

FREQUENCY CARACTERISTICS

PHASE CARACTERISTICS
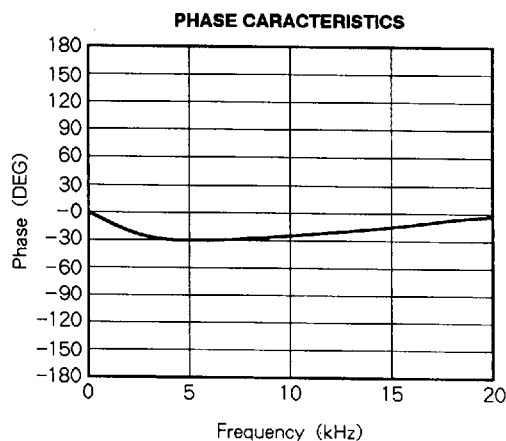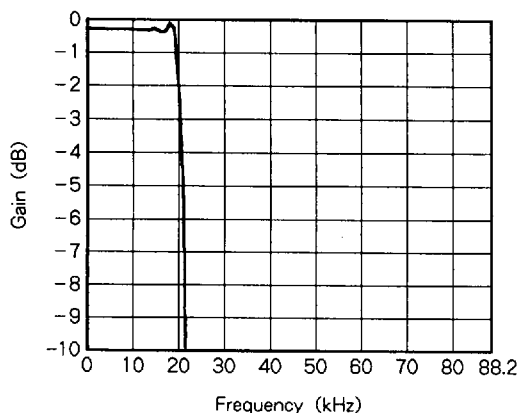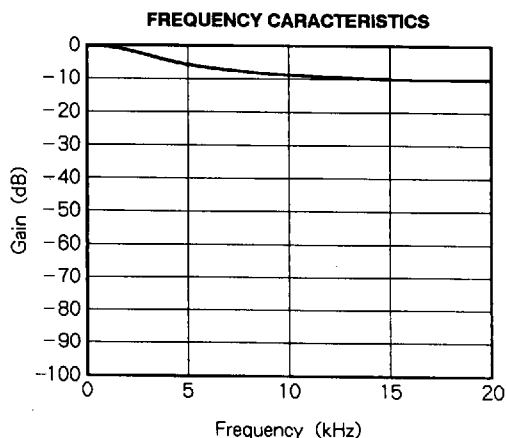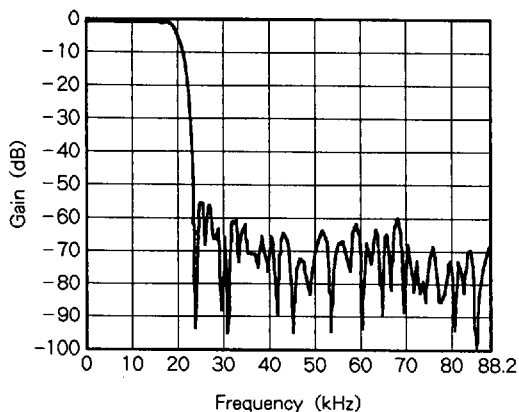
Fig. 4 Characteristic curve of digital filter

Ripple in pass band	Transient band	Attennation level in reduction band
≤ ± 0.15dB	20kHz to 24.1kHz	≤ − 53dB

Frequency	Deviation
0 to 18kHz	≤ ± 0.2dB
18 to 20kHz	≤ ± 0.5dB

10. MUTE CONTROL

(1) Zero cross muting

In the MUTE command is input from the microcomputer, the timing (zero-cross) at which the highest bit changes from "0" to "1" or "1" to "0" is detected, actuating the mute circuit. If zero cross cannot be detected within the specified time, the internal counter counts 34.8msec, forcedly actuating the mute circuit.

If the ZCRC register is set to "1", zero cross is forcedly muted with the MUTE command regardless of the presence or absence of zero cross.

(2) Attenuation control

If the ATT register is set to "1", the audio output is transmitted with −12dB down.

(3) Automatic fade mute

If the FMCNT register is set to "1", and the FMUTE register setting is changed from "0" to "1", the internal counter operates and the audio data fades in. This data fades out by changing FMUTE register setting from "1" to "0"

Two types of fade time can be set by setting the FMTC register.

Since "FADE MUTE" operates with the level set by the attenuate register as standard, attention should be paid to the attenuate register condition before operation start.

Fade time

FMTC	Fade time
L	2.2sec
H	34.8msec

(4) Control by the attenuate register

If the FMUTE register is set at "1" with the FMCNT register at "0", the audio data attenuates according to the contents of attenuate register, which are shown in Table 2.

Attenuate register control is carried out in 8 bits independently for right (R) and left (L) channels according to the microcomputer interface mode.

As shown in Table 2, the attenuate register is set in 8 bits. However, control up to −96.3dB is available with internal processing.

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Table 1. Attenuation control

No	C0	C1	C2	C3	C4	C5	C6	C7	Attenuation (dB)	No	C0	C1	C2	C3	C4	C5	C6	C7	Attenuation (dB)
FF	1	1	1	1	1	1	1	1	− 0.27	CF	1	1	1	1	0	0	1	1	− 18.34
FE	0	1	1	1	1	1	1	1	− 0.56	CE	0	1	1	1	0	0	1	1	− 18.62
FD	1	0	1	1	1	1	1	1	− 0.86	CD	1	0	1	1	0	0	1	1	− 18.92
FC	0	0	1	1	1	1	1	1	− 1.16	CC	0	0	1	1	0	0	1	1	− 19.22
FB	1	1	0	1	1	1	1	1	− 1.48	CB	1	1	0	1	0	0	1	1	− 19.54
FA	0	1	0	1	1	1	1	1	− 1.80	CA	0	1	0	1	0	0	1	1	− 19.86
F9	1	0	0	1	1	1	1	1	− 2.14	C9	1	0	0	1	0	0	1	1	− 20.21
F8	0	0	0	1	1	1	1	1	− 2.50	C8	0	0	0	1	0	0	1	1	− 20.56
F7	1	1	1	0	1	1	1	1	− 2.87	C7	1	1	1	0	0	0	1	1	− 20.93
F6	0	1	1	0	1	1	1	1	− 3.25	C6	0	1	1	0	0	0	1	1	− 21.32
F5	1	0	1	0	1	1	1	1	− 3.66	C5	1	0	1	0	0	0	1	1	− 21.72
F4	0	0	1	0	1	1	1	1	− 4.08	C4	0	0	1	0	0	0	1	1	− 22.14
F3	1	1	0	0	1	1	1	1	− 4.53	C3	1	1	0	0	0	0	1	1	− 22.59
F2	0	1	0	0	1	1	1	1	− 5.00	C2	0	1	0	0	0	0	1	1	− 23.06
F1	1	0	0	0	1	1	1	1	− 5.49	C1	1	0	0	0	0	0	1	1	− 23.56
F0	0	0	0	0	1	1	1	1	− 6.02	C0	0	0	0	0	0	0	1	1	− 24.08
EF	1	1	1	1	0	1	1	1	− 6.30	BF	1	1	1	1	1	1	0	1	− 24.39
EE	0	1	1	1	0	1	1	1	− 6.58	BE	0	1	1	1	1	1	0	1	− 24.64
ED	1	0	1	1	0	1	1	1	− 6.88	BD	1	0	1	1	1	1	0	1	− 24.94
EC	0	0	1	1	0	1	1	1	− 7.18	BC	0	0	1	1	1	1	0	1	− 25.24
EB	1	1	0	1	0	1	1	1	− 7.50	BB	1	1	0	1	1	1	0	1	− 25.56
EA	0	1	0	1	0	1	1	1	− 7.82	BA	0	1	0	1	1	1	0	1	− 25.89
E9	1	0	0	1	0	1	1	1	− 8.16	B9	1	0	0	1	1	1	0	1	− 26.22
E8	0	0	0	1	0	1	1	1	− 8.52	B8	0	0	0	1	1	1	0	1	− 26.58
E7	1	1	1	0	0	1	1	1	− 8.89	B7	1	1	1	0	1	1	0	1	− 26.95
E6	0	1	1	0	0	1	1	1	− 9.28	B6	0	1	1	0	1	1	0	1	− 27.34
E5	1	0	1	0	0	1	1	1	− 9.68	B5	1	0	1	0	1	1	0	1	− 27.74
E4	0	0	1	0	0	1	1	1	− 10.10	B4	0	0	1	0	1	1	0	1	− 28.16
E3	1	1	0	0	0	1	1	1	− 10.55	B3	1	1	0	0	1	1	0	1	− 28.61
E2	0	1	0	0	0	1	1	1	− 11.02	B2	0	1	0	0	1	1	0	1	− 29.08
E1	1	0	0	0	0	1	1	1	− 11.51	B1	1	0	0	0	1	1	0	1	− 29.58
E0	0	0	0	0	0	1	1	1	− 12.04	B0	0	0	0	0	1	1	0	1	− 30.10
DF	1	1	1	1	1	0	1	1	− 12.32	AF	1	1	1	1	0	1	0	1	− 30.38
DE	0	1	1	1	1	0	1	1	− 12.60	AE	0	1	1	1	0	1	0	1	− 30.66
DD	1	0	1	1	1	0	1	1	− 12.90	AD	1	0	1	1	0	1	0	1	− 30.96
DC	0	0	1	1	1	0	1	1	− 13.20	AC	0	0	1	1	0	1	0	1	− 31.26
DB	1	1	0	1	1	0	1	1	− 13.52	AB	1	1	0	1	0	1	0	1	− 31.58
DA	0	1	0	1	1	0	1	1	− 13.84	AA	0	1	0	1	0	1	0	1	− 31.91
D9	1	0	0	1	1	0	1	1	− 14.19	A9	1	0	0	1	0	1	0	1	− 32.25
D8	0	0	0	1	1	0	1	1	− 14.54	A8	0	0	0	1	0	1	0	1	− 32.60
D7	1	1	1	0	1	0	1	1	− 14.91	A7	1	1	1	0	0	1	0	1	− 32.97
D6	0	1	1	0	1	0	1	1	− 15.29	A6	0	1	1	0	0	1	0	1	− 33.36
D5	1	0	1	0	1	0	1	1	− 15.70	A5	1	0	1	0	0	1	0	1	− 33.76
D4	0	0	1	0	1	0	1	1	− 16.12	A4	0	0	1	0	0	1	0	1	− 34.19
D3	1	1	0	0	1	0	1	1	− 16.57	A3	1	1	0	0	0	1	0	1	− 34.63
D2	0	1	0	0	1	0	1	1	− 17.04	A2	0	1	0	0	0	1	0	1	− 35.10
D1	1	0	0	0	1	0	1	1	− 17.54	A1	1	0	0	0	0	1	0	1	− 35.60
D0	0	0	0	0	1	0	1	1	− 18.06	A0	0	0	0	0	0	1	0	1	− 36.12

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Table 1. Attenuation control (Continued)

No	C0	C1	C2	C3	C4	C5	C6	C7	Attenuation (dB)	No	C0	C1	C2	C3	C4	C5	C6	C7	Attenuation (dB)
9F	1	1	1	1	1	0	0	1	− 36.40	6F	1	1	1	1	0	1	1	0	− 54.46
9E	0	1	1	1	1	0	0	1	− 36.68	6E	0	1	1	1	0	1	1	0	− 54.75
9D	1	0	1	1	1	0	0	1	− 36.98	6D	1	0	1	1	0	1	1	0	− 55.04
9C	0	0	1	1	1	0	0	1	− 37.28	6C	0	0	1	1	0	1	1	0	− 55.34
9B	1	1	0	1	1	0	0	1	− 37.60	6B	1	1	0	1	0	1	1	0	− 55.66
9A	0	1	0	1	1	0	0	1	− 37.93	6A	0	1	0	1	0	1	1	0	− 55.99
99	1	0	0	1	1	0	0	1	− 38.27	69	1	0	0	1	0	1	1	0	− 56.33
98	0	0	0	1	1	0	0	1	− 36.62	68	0	0	0	1	0	1	1	0	− 56.68
97	1	1	1	0	1	0	0	1	− 38.99	67	1	1	1	0	0	1	1	0	− 57.05
96	0	1	1	0	1	0	0	1	− 39.38	66	0	1	1	0	0	1	1	0	− 57.44
95	1	0	1	0	1	0	0	1	− 39.78	65	1	0	1	0	0	1	1	0	− 57.84
94	0	0	1	0	1	0	0	1	− 40.21	64	0	0	1	0	0	1	1	0	− 58.27
93	1	1	0	0	1	0	0	1	− 40.65	63	1	1	0	0	0	1	1	0	− 58.71
92	0	1	0	0	1	0	0	1	− 41.12	62	0	1	0	0	0	1	1	0	− 59.18
91	1	0	0	0	1	0	0	1	− 41.62	61	1	0	0	0	0	1	1	0	− 59.68
90	0	0	0	0	1	0	0	1	− 42.14	60	0	0	0	0	0	1	1	0	− 60.21
8F	1	1	1	1	0	0	0	1	− 42.42	5F	1	1	1	1	1	0	1	0	− 60.48
8E	0	1	1	1	0	0	0	1	− 42.70	5E	0	1	1	1	1	0	1	0	− 60.77
8D	1	0	1	1	0	0	0	1	− 43.00	5D	1	0	1	1	1	0	1	0	− 61.06
8C	0	0	1	1	0	0	0	1	− 43.30	5C	0	0	1	1	1	0	1	0	− 61.37
8B	1	1	0	1	0	0	0	1	− 43.62	5B	1	1	0	1	1	0	1	0	− 61.68
8A	0	1	0	1	0	0	0	1	− 43.95	5A	0	1	0	1	1	0	1	0	− 62.01
89	1	0	0	1	0	0	0	1	− 44.29	59	1	0	0	1	1	0	1	0	− 62.35
88	0	0	0	1	0	0	0	1	− 44.64	58	0	0	0	1	1	0	1	0	− 62.70
87	1	1	1	0	0	0	0	1	− 45.01	57	1	1	1	0	1	0	1	0	− 63.07
86	0	1	1	0	0	0	0	1	− 45.40	56	0	1	1	0	1	0	1	0	− 63.46
85	1	0	1	0	0	0	0	1	− 45.80	55	1	0	1	0	1	0	1	0	− 63.86
84	0	0	1	0	0	0	0	1	− 46.23	54	0	0	1	0	1	0	1	0	− 64.28
83	1	1	0	0	0	0	0	1	− 46.67	53	1	1	0	0	1	0	1	0	− 64.73
82	0	1	0	0	0	0	0	1	− 47.14	52	0	1	0	0	1	0	1	0	− 65.20
81	1	0	0	0	0	0	0	1	− 47.64	51	1	0	0	0	1	0	1	0	− 65.70
80	0	0	0	0	0	0	0	1	− 48.16	50	0	0	0	0	1	0	1	0	− 66.22
7F	1	1	1	1	0	1	1	1	− 48.44	4F	1	1	1	1	0	0	1	0	− 66.50
7E	0	1	1	1	0	1	1	1	− 48.73	4E	0	1	1	1	0	0	1	0	− 66.79
7D	1	0	1	1	0	1	1	1	− 49.02	4D	1	0	1	1	0	0	1	0	− 67.08
7C	0	0	1	1	0	1	1	1	− 49.32	4C	0	0	1	1	0	0	1	0	− 67.39
7B	1	1	0	1	0	1	1	1	− 49.64	4B	1	1	0	1	0	0	1	0	− 67.70
7A	0	1	0	1	0	1	1	1	− 49.96	4A	0	1	0	1	0	0	1	0	− 68.03
79	1	0	0	1	0	1	1	1	− 50.31	49	1	0	0	1	0	0	1	0	− 68.37
78	0	0	0	1	0	1	1	1	− 50.66	48	0	0	0	1	0	0	1	0	− 68.73
77	1	1	1	0	0	1	1	1	− 51.03	47	1	1	1	0	0	0	1	0	− 69.10
76	0	1	1	0	0	1	1	1	− 51.42	46	0	1	1	0	0	0	1	0	− 69.48
75	1	0	1	0	0	1	1	1	− 51.82	45	1	0	1	0	0	0	1	0	− 69.89
74	0	0	1	0	0	1	1	1	− 52.25	44	0	0	1	0	0	0	1	0	− 70.31
73	1	1	0	0	0	1	1	1	− 52.69	43	1	1	0	0	0	0	1	0	− 70.75
72	0	1	0	0	0	1	1	1	− 53.16	42	0	1	0	0	0	0	1	0	− 71.22
71	1	0	0	0	0	1	1	1	− 53.66	41	1	0	0	0	0	0	1	0	− 71.72
70	0	0	0	0	0	1	1	1	− 54.18	40	0	0	0	0	0	0	1	0	− 72.25

Table 1. Attenuation control (Continued)

No	C0	C1	C2	C3	C4	C5	C6	C7	Attenuation (dB)	No	C0	C1	C2	C3	C4	C5	C6	C7	Attenuation (dB)
3F	1	1	1	1	1	1	0	0	−72.81	1F	1	1	1	1	1	0	0	0	−86.79
3E	0	1	1	1	1	1	0	0	−72.81	1E	0	1	1	1	1	0	0	0	−86.79
3D	1	0	1	1	1	1	0	0	−73.41	1D	1	0	1	1	1	0	0	0	−86.79
3C	0	0	1	1	1	1	0	0	−73.41	1C	0	0	1	1	1	0	0	0	−86.79
3B	1	1	0	1	1	1	0	0	−74.05	1B	1	1	0	1	1	0	0	0	−86.79
3A	0	1	0	1	1	1	0	0	−74.05	1A	0	1	0	1	1	0	0	0	−86.79
39	1	0	0	1	1	1	0	0	−74.75	19	1	0	0	1	1	0	0	0	−86.79
38	0	0	0	1	1	1	0	0	−74.75	18	0	0	0	1	1	0	0	0	−86.79
37	1	1	1	0	1	1	0	0	−75.50	17	1	1	1	0	1	0	0	0	−91.31
36	0	1	1	0	1	1	0	0	−75.50	16	0	1	1	0	1	0	0	0	−91.31
35	1	0	1	0	1	1	0	0	−76.32	15	1	0	1	0	1	0	0	0	−91.31
34	0	0	1	0	1	1	0	0	−76.32	14	0	0	1	0	1	0	0	0	−91.31
33	1	1	0	0	1	1	0	0	−77.24	13	1	1	0	0	1	0	0	0	−91.31
32	0	1	0	0	1	1	0	0	−77.24	12	0	1	0	0	1	0	0	0	−91.31
31	1	0	0	0	1	1	0	0	−78.26	11	1	0	0	0	1	0	0	0	−91.31
30	0	0	0	0	1	1	0	0	−78.26	10	0	0	0	0	1	0	0	0	−91.31
2F	1	1	1	1	0	1	0	0	−79.43	0F	1	1	1	1	0	0	0	0	−96.33
2E	0	1	1	1	0	1	0	0	−79.43	0E	0	1	1	1	0	0	0	0	−96.33
2D	1	0	1	1	0	1	0	0	−79.43	0D	1	0	1	1	0	0	0	0	−96.33
2C	0	0	1	1	0	1	0	0	−79.43	0C	0	0	1	1	0	0	0	0	−96.33
2B	1	1	0	1	0	1	0	0	−80.77	0B	1	1	0	1	0	0	0	0	−96.33
2A	0	1	0	1	0	1	0	0	−80.77	0A	0	1	0	1	0	0	0	0	−96.33
29	1	0	0	1	0	1	0	0	−80.77	09	1	0	0	1	0	0	0	0	−96.33
28	0	0	0	1	0	1	0	0	−80.77	08	0	0	0	1	0	0	0	0	−96.33
27	1	1	1	0	0	1	0	0	−82.35	07	1	1	1	0	0	0	0	0	−96.33
26	0	1	1	0	0	1	0	0	−82.35	06	0	1	1	0	0	0	0	0	−96.33
25	1	0	1	0	0	1	0	0	−82.35	05	1	0	1	0	0	0	0	0	−96.33
24	0	0	1	0	0	1	0	0	−82.35	04	0	0	1	0	0	0	0	0	−96.33
23	1	1	0	0	0	1	0	0	−84.29	03	1	1	0	0	0	0	0	0	−96.33
22	0	1	0	0	0	1	0	0	−84.29	02	0	1	0	0	0	0	0	0	−96.33
21	1	0	0	0	0	1	0	0	−84.29	01	1	0	0	0	0	0	0	0	−96.33
20	0	0	0	0	0	1	0	0	−84.29	00	0	0	0	0	0	0	0	0	−∞

11. DIGITAL SILENCE

When SIL/EST bit of the status register is in "L" if the audio data meets the following requirements, the computer regards the current condition as silent, and a silence single is output from RSIL/EST1 & RSIL/EST2 pins.

(Silence Conditions)

[If the sudio data is hexadecimal, and the period of "0000" or "FFFF" continues for at least 200msec, the current condition is regarded as silent. However, if "0000" and "FFFF" are displayed alternately even once within 200msec, it is not regarded as silence.]

Rch silence information and Lch silence information are output from RSIL/EST1 and LSIL/EST2 pins respectively. If both pins are judged to be silent, "L" is output.

When SIL/EST bit is in "H", the pin becomes an error monitor pin for error correction ; C1 error and C2 error are output from RSIL/EST1 and LSIL/EST2 pins respectively.

When SILC bit is in "L", silence information is output independently for R & L channels as explained above.

When SILC bit is in "H", silence information is output from RSIL/EST1 pin if both Lch and Rch audio data sre placed in the silent state.
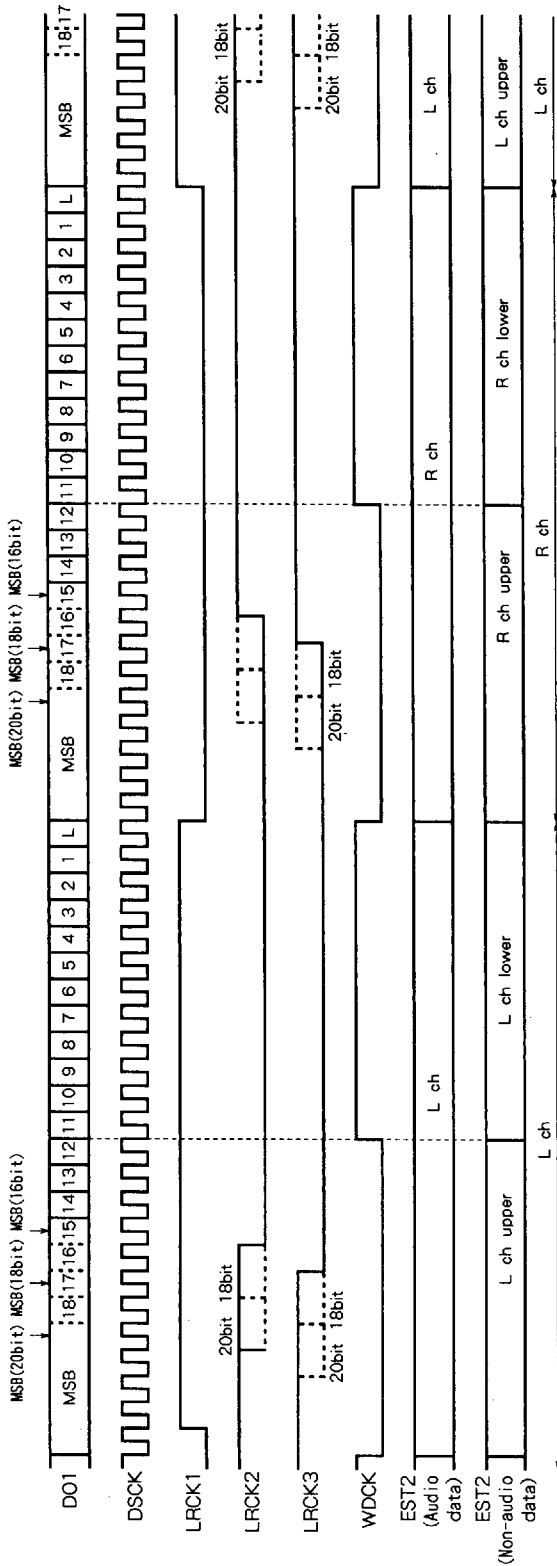
12. DAC INTERFACE

(1) DAC interface mode table

No.	Register name					Operation	Fs
	NON-AUDIO	DFPAS	18BIT	20BIT	DUAL-DAC		
1	L	L	L	L	L	16-bit single DAC	4Fs
2	L	L	L	L	H	16-bit dual DAC	4Fs
3	L	L	H	L	L	18-bit single DAC	4Fs
4	L	L	H	L	H	18-bit dual DAC	4Fs
5	L	L	L	H	L	20-bit single DAC	4Fs
6	L	L	L	H	H	20-bit dual DAC	4Fs
7	L	H	L	L	L	16-bit single DAC	Fs
8	H	H	L	L	L	Non-audio mode	Fs

(2) Stereo/Monaural mode selection

Register name		Operation
LMONO	RMONO	
L	L	Stereo output
H	L	Lch monoural output
L	H	Rch monoural output
H	H	Inhibit

(3) DAC interface time chart

(3-1)Single DAC mode

DO1

DSCK

LRCK1

LRCK2

LRCK3

WDCK

EST2 (Audio data)

EST2 (Non-audio data)

MSB(20bit) MSB(18bit) MSB(16bit)

MSB

20bit 18bit

20bit 18bit

L ch upper

L ch lower

L ch

L ch

R ch upper

R ch lower

R ch

R ch

MSB(20bit) MSB(18bit) MSB(16bit)

MSB

20bit 18bit

20bit 18bit

L ch

L ch upper

L ch

(3-2)Dual DAC Mode

DO1(Lch)

DO2(Rch)

DSCK

LRCK1

LRCK2

LRCK3

MSB(20bit) MSB(18bit) MSB(16bit)

MSB

MSB

18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 L

18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 L

20bit 18bit 16bit

20bit 18bit 16bit

20bit 18bit 16bit

13 OSCILLATION CIRCUIT

(1) Self-oscillation circuit

An oscillation circuit can be formed by connecting a 8.4672 MHz or 16.9344MHz crystal oscillator and loading to pins X_1, X_0.

8.4672 (16.9344MHz) shaped from this oscillator is output to C846 pin, and 4.2336MHz (8.4672MHz) divided and generated is output to C423 pin.

The oscillation frequency is selected as follows, using CKSEL pin :

Vibrator	CKSEL	Remarks
8.4672MHz	H	Normal playback mode
16.9344MHz	L	
16.9344MHz	H	Double speed playback mode

Vibrator	Load capacity value (Reference)
8.4672MHz	30pF
16.9344MHz	15pF
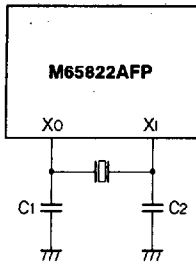
(2) When external clock is used

If an 8.4672MHz or 16.9344MHz clock is present inside the system, the data can be input through the capacitor to pin X_1 without using a crystal vibrator. (No capacitor is required if the input level corresponds to a logic level.)

The selection of a vibrator according to the crystal clock output and CKSEL pin is the same as in self-oscillation.
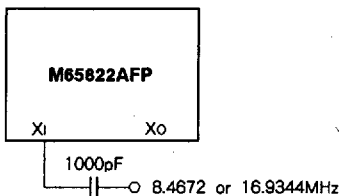
External clock	Min.	Max.
V_{IH}	GND	V_{DD}
Amplitude	$1V_{P-P}$	–

MITSUBISHI ELECTRIC

CD PLAYER DIGITAL SIGNAL PROCESSOR

APPLICATION EXAMPLE