CMOS LSI

LC72133M, 72133V

PLL Frequency Synthesizer for Electronic Tuning

Overview

The LC72133M and LC72133V are a phase-locked loop frequency synthesizer LSI circuits for use in radio tuners. It supports low-voltage (2.7 to 3.6 V) operation and can implement high-performance AM/FM tuners easily.

Functions

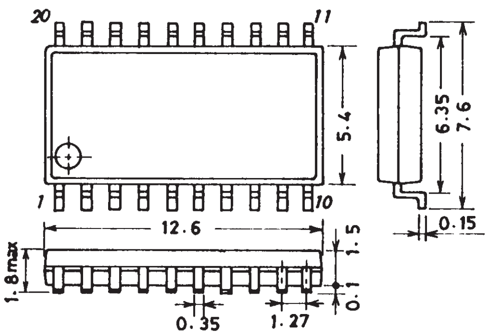
- High speed programmable dividers
  - FMIN: 10 to 120 MHz ....pulse swallower (built-in divide-by-two prescaler), $V_{DD} \geq 2.7$ V
    10 to 130 MHz ....pulse swallower (built-in divide-by-two prescaler), $V_{DD} \geq 3.0$ V
  - AMIN: 2 to 40 MHz ....pulse swallower
    0.5 to 10 MHz ....direct division
- IF counter
  - IFIN: 0.4 to 12 MHz ....AM/FM IF counter
- Reference frequencies
  - Twelve selectable frequencies (4.5 or 7.2 MHz crystal)
    1, 3, 5, 9, 10, 3.125, 6.25, 12.5, 15, 25, 50 and 100 kHz
- Phase comparator
  - Dead zone control
  - Unlock detection circuit
  - Deadlock clear circuit
- Built-in MOS transistor for forming an active low-pass filter
- I/O ports
  - Dedicated output ports: 4
  - Input or output ports: 2
  - Support clock time base output
- Serial data I/O
  - Support CCB format communication with the system controller.
- Operating ranges
  - Supply voltage........................2.7 to 3.6 V
  - Operating temperature............–20 to +70°C
- Package
  MFP20
  SSOP20

Package Dimensions

unit: mm

3036B-MFP20

[LC72133M]

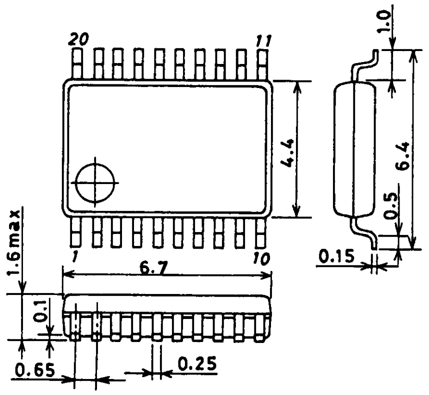


SANYO: MFP20

unit: mm

3179A-SSOP20

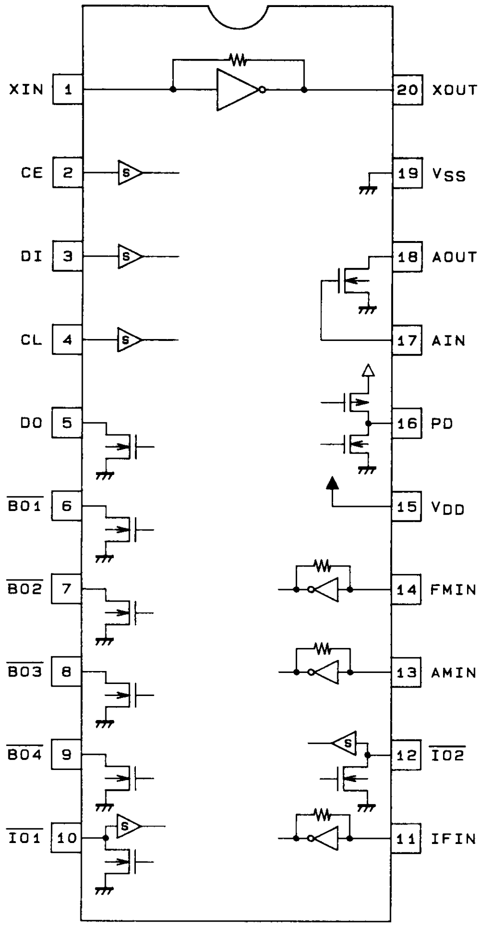
[LC72133V]



SANYO: SSOP20

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Pin Assignment



Top view

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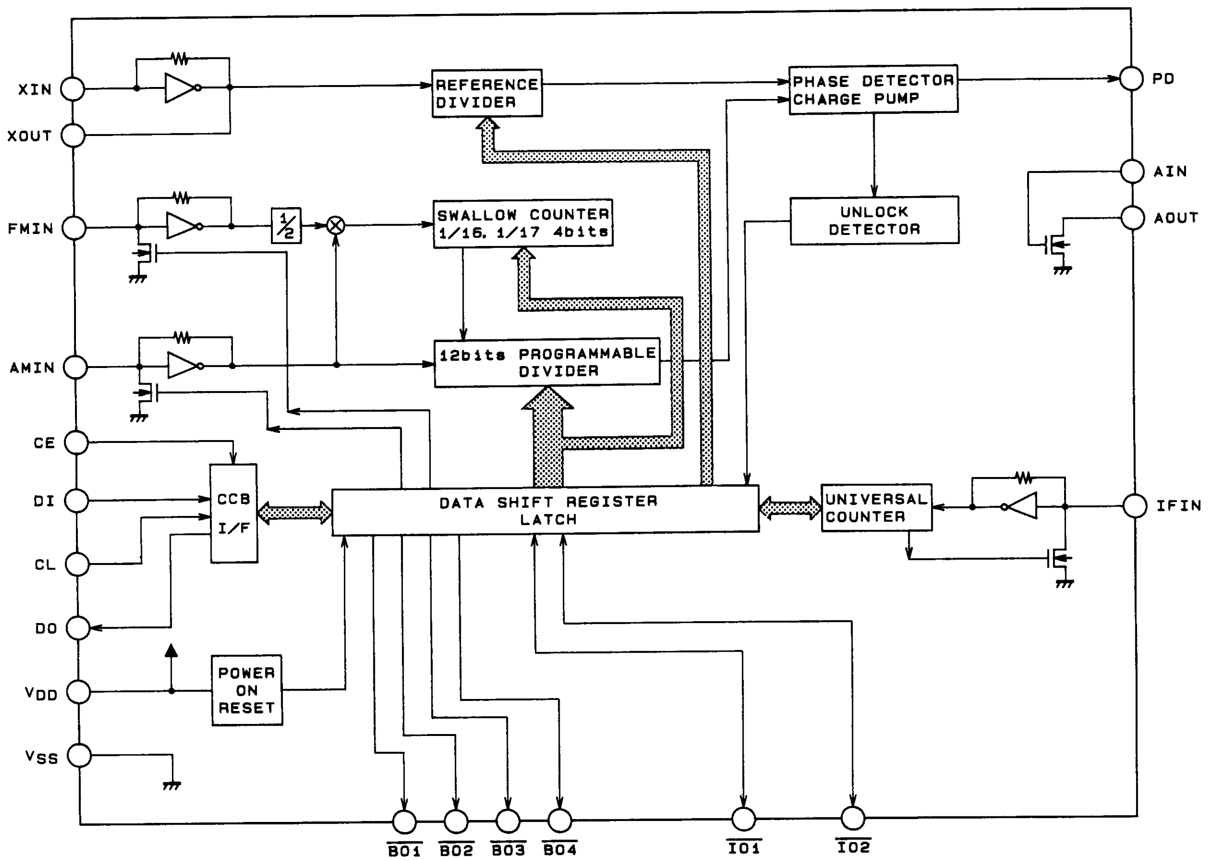
Block Diagram



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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

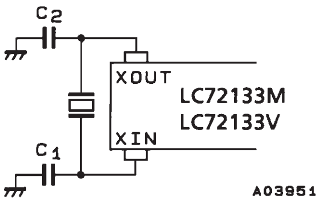
Parameter	Symbol	Pins	Ratings	Unit
Supply voltage	V_{DD} max	V_{DD}	–0.3 to +5.5	V
Maximum input voltage	$V_{IN}1$ max	CE, CL, DI, AIN	–0.3 to +5.5	V
	$V_{IN}2$ max	XIN, FMIN, AMIN, IFIN	–0.3 to V_{DD} + 0.3	V
	$V_{IN}3$ max	$\overline{\text{IO1}}$, $\overline{\text{IO2}}$	–0.3 to +15	V
Maximum output voltage	V_O1 max	DO	–0.3 to +5.5	V
	V_O2 max	XOUT, PD	–0.3 to V_{DD} + 0.3	V
	V_O3 max	$\overline{\text{BO1}}$ to $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$, AOUT	–0.3 to +15	V
Maximum output current	I_O1 max	BO1	0 to 3.0	mA
	I_O2 max	AOUT, DO	0 to 6.0	mA
	I_O3 max	$\overline{\text{BO2}}$ to $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$	0 to 6.0	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C: LC72133M	180	mW
		Ta ≤ 70°C: LC72133V	160	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –20 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}		2.7		3.6	V
Input high-level voltage	$V_{IH}1$	CE, CL, DI		0.7 V_{DD}		5.5	V
	$V_{IH}2$	$\overline{\text{IO1}}$, $\overline{\text{IO2}}$		0.7 V_{DD}		13	V
Input low-level voltage	V_{IL}	CE, CL, DI, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$		0		0.3 V_{DD}	V
Output voltage	V_O1	DO		0		5.5	V
	V_O2	$\overline{\text{BO1}}$ to $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$, AOUT		0		13	V
Input frequency	$f_{IN}1$	XIN	$V_{IN}1$	1		8	MHz
	$f_{IN}2\text{-}1$	FMIN	$V_{IN}2\text{-}1$	10		90	MHz
	$f_{IN}2\text{-}2$	FMIN	$V_{IN}2\text{-}2$	10		120	MHz
	$f_{IN}2\text{-}3$	FMIN	$V_{IN}2\text{-}1$, V_{DD} ≥ 3.0 V	10		130	MHz
	$f_{IN}3$	AMIN	$V_{IN}3$, SNS = 1	2		40	MHz
	$f_{IN}4$	AMIN	$V_{IN}4$, SNS = 0	0.5		10	MHz
	$f_{IN}5$	IFIN	$V_{IN}5$	0.4		12	MHz
Input amplitude	$V_{IN}1$	XIN	$f_{IN}1$	400		900	mVrms
	$V_{IN}2\text{-}1$	FMIN	$f_{IN}2\text{-}1$, $f_{IN}2\text{-}3$	70		900	mVrms
	$V_{IN}2\text{-}2$	FMIN	$f_{IN}2\text{-}2$	100		900	mVrms
	$V_{IN}3$	AMIN	$f_{IN}3$, SNS = 1	70		900	mVrms
	$V_{IN}4$	AMIN	$f_{IN}4$, SNS = 0	70		900	mVrms
	$V_{IN}5\text{-}1$	IFIN	$f_{IN}5$, IFS = 1	70		900	mVrms
	$V_{IN}5\text{-}2$	IFIN	$f_{IN}6$, IFS = 0	100		900	mVrms
Supported crystals	Xtal	XIN, XOUT	*	4.0		8.0	MHz

Note: * Recommended crystal oscillator CI values:
CI ≤ 120Ω (For a 4.5 MHz crystal)
CI ≤ 70Ω (For a 7.2 MHz crystal)

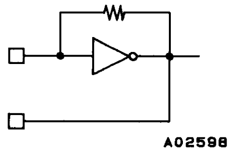
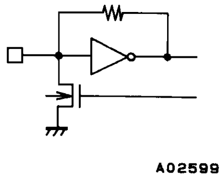
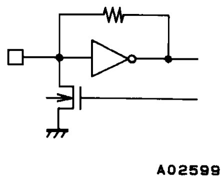
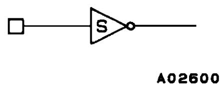
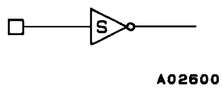
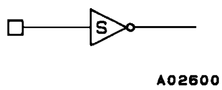
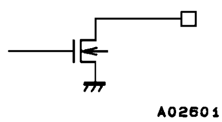
<Sample Oscillator Circuit>
Crystal oscillator: HC-49/U (manufactured by Kinseki, Ltd.), CL = 12 pF
C1 = C2 = 15 pF
The circuit constants for the crystal oscillator circuit depend on the crystal used, the printed circuit board pattern, and other items. Therefore we recommend consulting with the manufacturer of the crystal for evaluation and reliability.



Electrical Characteristics for the Allowable Operating Ranges at Ta = –20 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Built-in feedback resistance	Rf1	XIN			1.0		MΩ
	Rf2	FMIN			500		kΩ
	Rf3	AMIN			500		kΩ
	Rf4	IFIN			250		kΩ
Built-in pull-down resistor	Rpd1	FMIN			200		kΩ
	Rpd2	AMIN			200		kΩ
Hysteresis	V_{HIS}	CE, CL, DI, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$			0.1 V_{DD}		V
Output high level voltage	$V_{OH}1$	PD	I_O = –1 mA	V_{DD} – 1.0			V
Output low level voltage	$V_{OL}1$	PD	I_O = 1 mA			1.0	V
	$V_{OL}2$	$\overline{\text{BO1}}$	I_O = 0.5 mA			0.6	V
			I_O = 1 mA			1.2	V
	$V_{OL}3$	DO	I_O = 1 mA			0.25	V
			I_O = 3 mA			0.75	V
	$V_{OL}4$	$\overline{\text{BO2}}$ to $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$	I_O = 1 mA			0.25	V
			I_O = 5 mA			1.25	V
	$V_{OL}5$	AOUT	I_O = 1 mA, AIN = 1.3 V			0.5	V
Input high level current	$I_{IH}1$	CE, CL, DI	V_I = 5.5 V			5.0	µA
	$I_{IH}2$	$\overline{\text{IO1}}$, $\overline{\text{IO2}}$	V_I = 13 V			5.0	µA
	$I_{IH}3$	XIN	$V_I = V_{DD}$	1.3		8	µA
	$I_{IH}4$	FMIN, AMIN	$V_I = V_{DD}$	2.7		15	µA
	$I_{IH}5$	IFIN	$V_I = V_{DD}$	5.4		30	µA
	$I_{IH}6$	AIN	V_I = 5.5 V			200	nA
Input low level current	$I_{IL}1$	CE, CL, DI	V_I = 0 V			5.0	µA
	$I_{IL}2$	$\overline{\text{IO1}}$, $\overline{\text{IO2}}$	V_I = 0 V			5.0	µA
	$I_{IL}3$	XIN	V_I = 0 V	1.3		8	µA
	$I_{IL}4$	FMIN, AMIN	V_I = 0 V	2.7		15	µA
	$I_{IL}5$	IFIN	V_I = 0 V	5.4		30	µA
	$I_{IL}6$	AIN	V_I = 0 V			200	nA
Output off leakage current	$I_{OFF}1$	$\overline{\text{BO1}}$ to $\overline{\text{BO4}}$, AOUT, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$	V_O = 13 V			5.0	µA
	$I_{OFF}2$	DO	V_O = 5.5 V			5.0	µA
High level three-state off leakage current	I_{OFFH}	PD	$V_O = V_{DD}$		0.01	200	nA
Low level three-state off leakage current	I_{OFFL}	PD	V_O = 0 V		0.01	200	nA
Input capacitance	C_{IN}	FMIN			6		pF
Current drain	$I_{DD}1$	V_{DD}	Xtal = 7.2 MHz, $f_{IN}2$ = 130 MHz, $V_{IN}2$ = 70 mVrms		2	5	mA
	$I_{DD}2$	V_{DD}	PLL block stopped (PLL INHIBIT), Xtal oscillator operating (Xtal = 7.2 MHz)		0.3		mA
	$I_{DD}3$	V_{DD}	PLL block stopped Xtal oscillator stopped			30	µA

Pin Functions

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Functions</th><th>Circuit configuration</th></tr>
<tr><td>XIN
XOUT</td><td>1
20</td><td>Xtal OSC</td><td>• Crystal resonator connection (4.5/7.2 MHz)</td><td></td></tr>
<tr><td>FMIN</td><td>14</td><td>Local oscillator signal input</td><td>• FMIN is selected when the serial data input DVS bit is set to 1.
• The input frequency range is from 10 to 130 MHz.
• The input signal passes through the internal divide-by-two prescaler and is input to the swallow counter.
• The divisor can be in the range 272 to 65535. However, since the signal has passed through the divide-by-two prescaler, the actual divisor is twice the set value.
<table>
<tr><td rowspan="2">Operating conditions</td><td colspan="3">FMIN input frequency</td></tr>
<tr><td>10 to 90 MHz</td><td>10 to 120 MHz</td><td>10 to 130 MHz</td></tr>
<tr><td>Operating power-supply voltage</td><td>2.7 to 3.6 V</td><td>2.7 to 3.6 V</td><td>3.0 to 3.6 V</td></tr>
<tr><td>Operating input levels</td><td>70 to 900 mVrms</td><td>100 to 900 mVrms</td><td>70 to 900 mVrms</td></tr>
</table></td><td></td></tr>
<tr><td>AMIN</td><td>13</td><td>Local oscillator signal input</td><td>• AMIN is selected when the serial data input DVS bit is set to 0.
• When the serial data input SNS bit is set to 1:
— The input frequency range is 2 to 40 MHz.
— The signal is directly input to the swallow counter.
— The divisor can be in the range 272 to 65535, and the divisor used will be the value set.
• When the serial data input SNS bit is set to 0:
— The input frequency range is 0.5 to 10 MHz.
— The signal is directly input to a 12-bit programmable divider.
— The divisor can be in the range 4 to 4095, and the divisor used will be the value set.</td><td></td></tr>
<tr><td>CE</td><td>2</td><td>Chip enable</td><td>Set this pin high when inputting (DI) or outputting (DO) serial data.</td><td></td></tr>
<tr><td>CL</td><td>4</td><td>Clock</td><td>• Used as the synchronization clock when inputting (DI) or outputting (DO) serial data.</td><td></td></tr>
<tr><td>DI</td><td>3</td><td>Data input</td><td>• Inputs serial data transferred from the controller to the LC72133.</td><td></td></tr>
<tr><td>DO</td><td>5</td><td>Data output</td><td>• Outputs serial data transferred from the LC72133 to the controller.
The content of the output data is determined by the serial data DOC0 to DOC2.</td><td></td></tr>
<tr><td>V_{DD}</td><td>15</td><td>Power supply</td><td>• The LC72133 power supply pin (V_{DD} = 2.7 to 3.6 V)
• The power on reset circuit operates when power is first applied.</td><td></td></tr>
</table>

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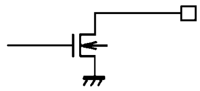
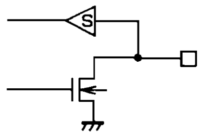
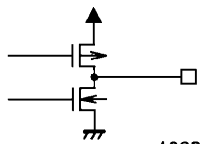
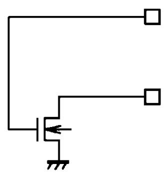
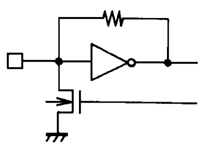
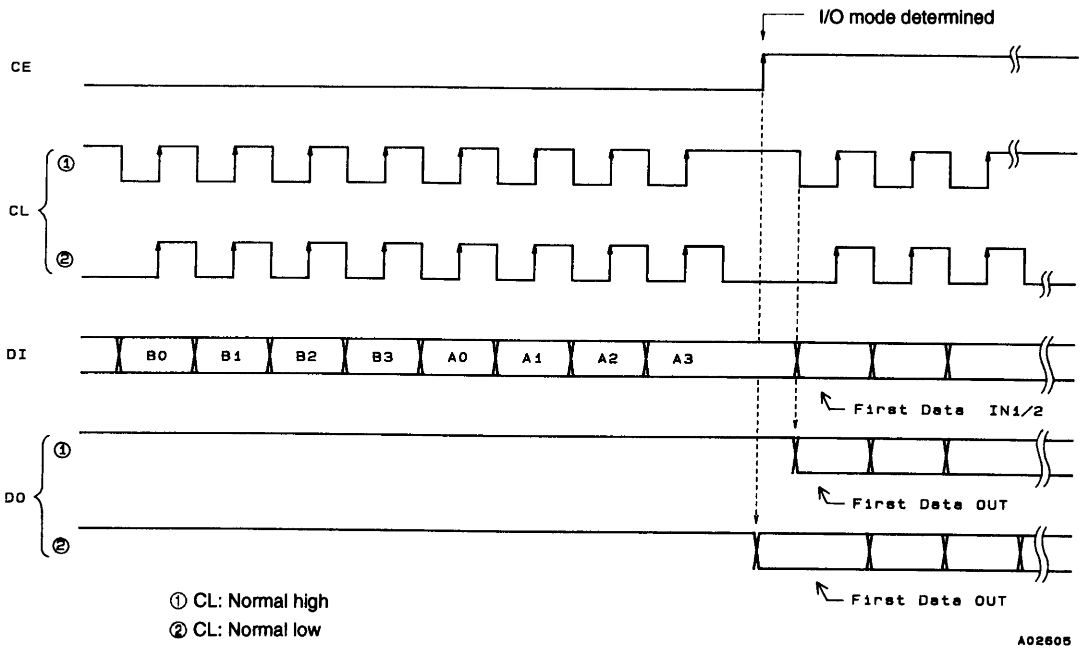
Symbol	Pin No.	Type	Functions	Circuit configuration
V_{SS}	19	Ground	• The LC72133 ground	—
$\overline{BO1}$ $\overline{BO2}$ $\overline{BO3}$ $\overline{BO4}$	6 7 8 9	Output port	• Dedicated output pins • The output states are determined by $\overline{BO1}$ to $\overline{BO4}$ bits in the serial data. Data: 0 = open, 1 = low • A time base signal (8 Hz) can be output from the $\overline{BO1}$ pin. (When the serial data TBC bit is set to 1.) • Care is required when using the $\overline{BO1}$ pin, since it has a higher on impedance than the other output ports (pins $\overline{BO2}$ to $\overline{BO4}$). • The data = 0 (open) state is selected after the power-on reset.	 A02601
$\overline{IO1}$ $\overline{IO2}$	10 12	I/O port	• I/O dual-use pins • The direction (input or output) is determined by bits IOC1 and IOC2 in the serial data. Data: 0 = input port, 1 = output port • When specified for use as input ports: The state of the input pin is transmitted to the controller over the DO pin. Input state: low = 0 data value high = 1 data value • When specified for use as output ports: The output states are determined by the IO1 and IO2 bits in the serial data. Data: 0 = open, 1 = low • These pins function as input pins following a power on reset.	 A02602
PD	16	Charge pump output	• PLL charge pump output When the frequency generated by dividing the local oscillator frequency by N is higher than the reference frequency, a high level is output from the PD pin. Similarly, when that frequency is lower, a low level is output. The PD pin goes to the high impedance state when the frequencies match.	 A02603
AIN AOUT	17 18	LPF amplifier transistor	• The n-channel MOS transistor used for the PLL active low-pass filter.	 A02604
IFIN	11	IF counter	• Accepts an input in the frequency range 0.4 to 12 MHz. • The input signal is directly transmitted to the IF counter. • The result is output starting the MSB of the IF counter using the DO pin. • Four measurement periods are supported: 4, 8, 32, and 64 ms.	 A02599

Serial Data I/O Methods

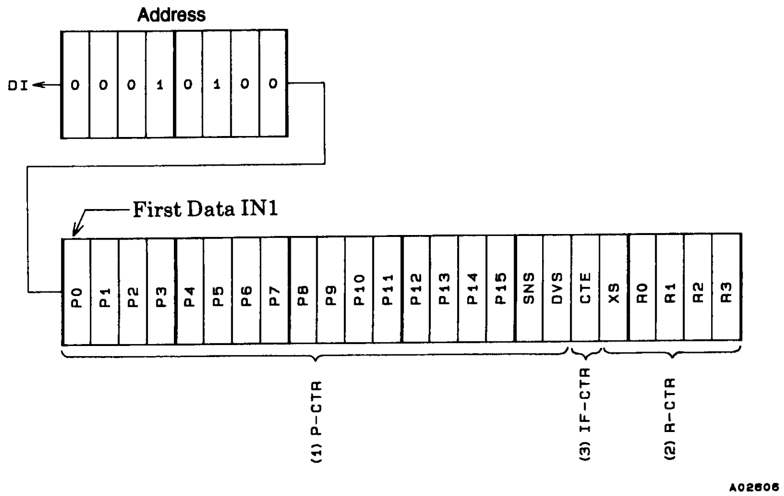
The LC72133 inputs and outputs data using the Sanyo CCB (computer control bus) audio LSI serial bus format. This LSI adopts an 8-bit address format CCB.

	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
1	IN1 (82)	0	0	0	1	0	1	0	0	• Control data input mode (serial data input) • 24 data bits are input. • See the "DI Control Data (serial data input) Structure" item for details on the meaning of the input data.
2	IN2 (92)	1	0	0	1	0	1	0	0	• Control data input mode (serial data input) • 24 data bits are input. • See the "DI Control Data (serial data input) Structure" item for details on the meaning of the input data.
3	OUT (A2)	0	1	0	1	0	1	0	0	Data output mode (serial data output) • The number of bits output is equal to the number of clock cycles. • See the "DO Output Data (Serial Data Output) Structure" item for details on the meaning of the output data.

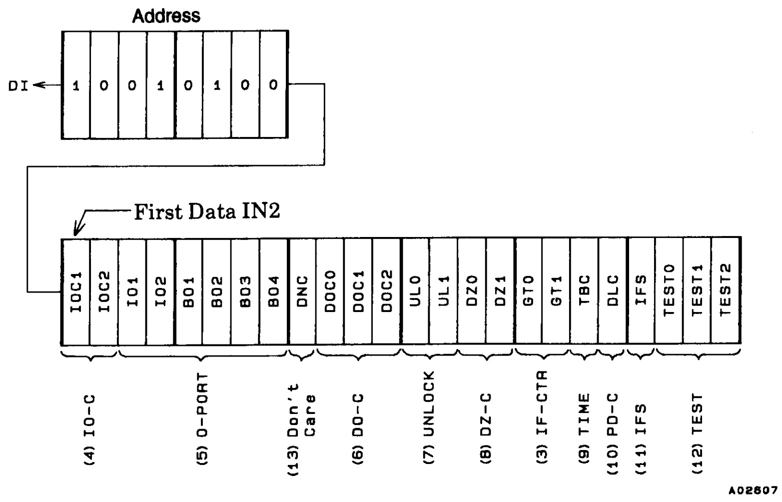


1. DI Control Data (Serial Data Input) Structure

- IN1 Mode



- IN2 Mode



2. DI Control Data Functions

<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15

DVS, SNS</td><td>• Data that sets the programmable divider.
A binary value in which P15 is the MSB. The LSB changes depending on DVS and SNS. (*: don’t care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th><th>Actual divisor</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the value of the setting</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The value of the setting</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The value of the setting</td></tr>
</table>
Note: P0 to P3 are ignored when P4 is the LSB.
• Selects the signal input pin (AMIN or FMIN) for the programmable divider, switches the input frequency range. (*: don’t care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 130 MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr>
</table>
Note: See the “Programmable Divider” item for more information.</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data
R0 to R3

XS</td><td>• Reference frequency (fref) selection data.
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency (kHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + Xtal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
Note: PLL INHIBIT
The programmable divider block and the IF counter block are stopped, the FMIN, AMIN, and IFIN pins are set to the pull-down state (ground), and the charge pump goes to the high impedance state.
• Crystal resonator selection
XS = 0: 4.5 MHz
XS = 1: 7.2 MHz
The 7.2 MHz frequency is selected after the power-on reset.</td><td></td></tr>
<tr><td>(3)</td><td>IF counter control data
CTE

GT0, GT1</td><td>• IF counter measurement start data
CTE = 1: Counter start
CTE = 0: Counter reset
• Determines the IF counter measurement period.
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time (ms)</th><th>Wait time (ms)</th></tr>
<tr><td>0</td><td>0</td><td>4</td><td>3 to 4</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td></tr>
</table>
Note: See the “IF Counter” item for more information.</td><td>IFS</td></tr>
<tr><td>(4)</td><td>I/O port specification data
IOC1, IOC2</td><td>• Specifies the I/O direction for the bidirectional pins $\overline{IO1}$ and $\overline{IO2}$.
Data: 0 = input mode, 1 = output mode</td><td></td></tr>
<tr><td>(5)</td><td>Output port data
BO1 to BO4, IO1, IO2</td><td>• Data that determines the output from the $\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$ and $\overline{IO2}$ output ports
Data: 0 = open, 1 = low
• The data = 0 (open) state is selected after the power-on reset.</td><td>IOC1
IOC2</td></tr>
</table>

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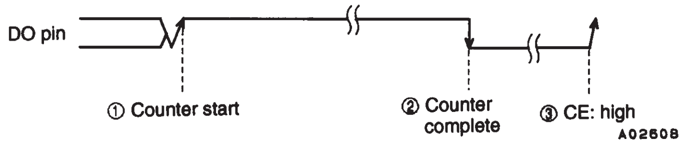
<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(6)</td><td>DO pin control data
DOC0, DOC1, DOC2</td><td>• Data that determines the DO pin output
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when the unlock state is detected</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC*1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>The $\overline{IO1}$ pin state*2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The IO2 pin state*2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
The open state is selected after the power-on reset.
Note: 1. end-UC: Check for IF counter measurement completion


① When end-UC is set and the IF counter is started (i.e., when CTE is changed from zero to one), the DO pin automatically goes to the open state.
② When the IF counter measurement completes, the DO pin goes low to indicate the measurement completion state.
③ Depending on serial data I/O (CE: high) the DO pin goes to the open state.
2. Goes to the open state if the I/O pin is specified to be an output port.
Caution: The state of the DO pin during a data input period (an IN1 or IN2 mode period with CE high) will be open, regardless of the state of the DO control data (DOC0 to DOC2). Also, the DO pin during a data output period (an OUT mode period with CE high) will output the contents of the internal DO serial data in synchronization with the CL pin signal, regardless of the state of the DO control data (DOC0 to DOC2).</td><td>UL0, UL1,
CTE,
IOC1, IOC2</td></tr>
<tr><td>(7)</td><td>Unlock detection data
UL0, UL1</td><td>• Selects the phase error (øE) detection width for checking PLL lock.
A phase error in excess of the specified detection width is seen as an unlocked state.
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detector output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>øE is output directly</td></tr>
<tr><td>1</td><td>0</td><td>±0.55 µs</td><td>øE is extended by 1 to 2 ms</td></tr>
<tr><td>1</td><td>1</td><td>±1.11</td><td>øE is extended by 1 to 2 ms</td></tr>
</table>
Note: In the unlocked state the DO pin goes low and the UL bit in the serial data becomes zero.</td><td>DOC0,
DOC1,
DOC2</td></tr>
<tr><td>(8)</td><td>Phase comparator control data
DZ0, DZ1</td><td>• Controls the phase comparator dead zone.
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
Dead zone widths: DZA < DZB < DZC < DZD</td><td></td></tr>
<tr><td>(9)</td><td>Clock time base
TBC</td><td>Setting $\overline{TBC}$ to one causes an 8 Hz, 40% duty clock time base signal to be output from the $\overline{BO1}$ pin. (BO1 data is invalid in this mode.)</td><td>BO1</td></tr>
<tr><td>(10)</td><td>Charge pump control data
DLC</td><td>• Forcibly controls the charge pump output.
<table>
<tr><th>DLC</th><th>Charge pump output</th></tr>
<tr><td>0</td><td>Normal operation</td></tr>
<tr><td>1</td><td>Forced low</td></tr>
</table>
Note: If deadlock occurs due to the VCO control voltage (Vtune) going to zero and the VCO oscillator stopping, deadlock can be cleared by forcing the charge pump output to low and setting Vtune to V_{CC}. (This is the deadlock clearing circuit.)</td><td></td></tr>
</table>

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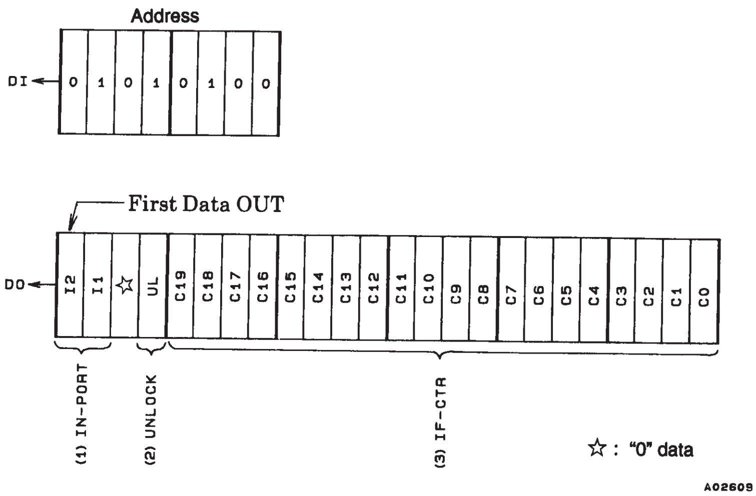
No.	Control block/data	Functions	Related data
(11)	IF counter control data IFS	• Note that if this value is set to zero the system enters input sensitivity degradation mode, and the sensitivity is reduced to 10 to 30 mV rms. * See the "IF Counter Operation" item for details.	
(12)	LSI test data TEST 0 to TEST 2	• LSI test data TEST0 TEST1 These values must all be set to 0. TEST2 These test data are set to 0 automatically after the power-on reset.	
(13)	DNC	Don't care. This data must be set to 0.	

3. DO Output Data (Serial Data Output)

• OUT Mode

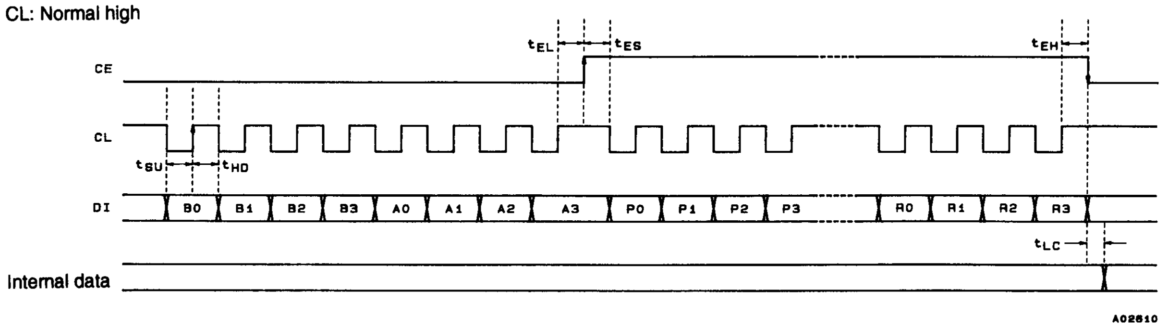


4. DO Output Data

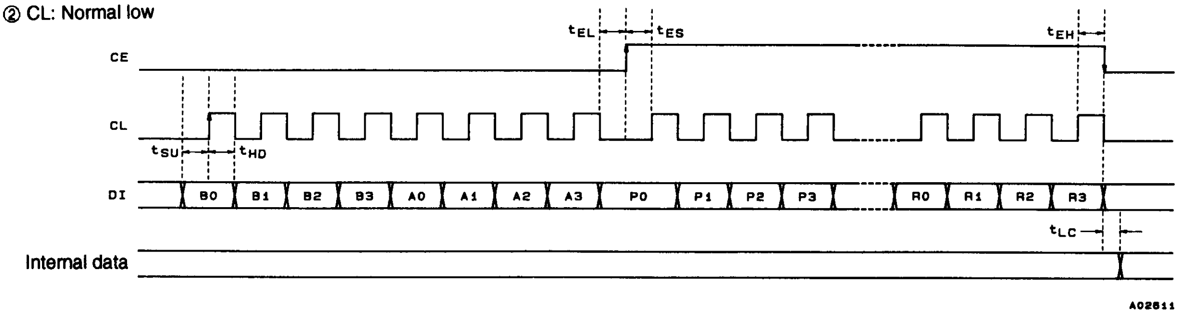
No.	Control block/data	Functions	Related data
(1)	I/O port data I2, I1	• Latched from the pin states of the $\overline{IO1}$ and $\overline{IO2}$ I/O ports. • These values follow the pin states regardless of the input or output setting. • Data is latched at the point where the circuit enters data output mode (OUT mode). I1 ← $\overline{IO1}$ pin state High: 1 I2 ← $\overline{IO2}$ pin state Low: 0	IOC1, IOC2
(2)	PLL unlock data UL	• Latched from the state of the unlock detection circuit. UL ← 0: Unlocked UL ← 1: Locked or detection stopped mode	UL0, UL1
(3)	IF counter binary data C19 to C0	• Latched from the value of the IF counter (20-bit binary counter). C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTE, GT0, GT1

5. Serial Data Input (IN1/IN2) t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} ≥ 0.75 μs, t_{LC} < 0.75 μs

① CL: Normal high

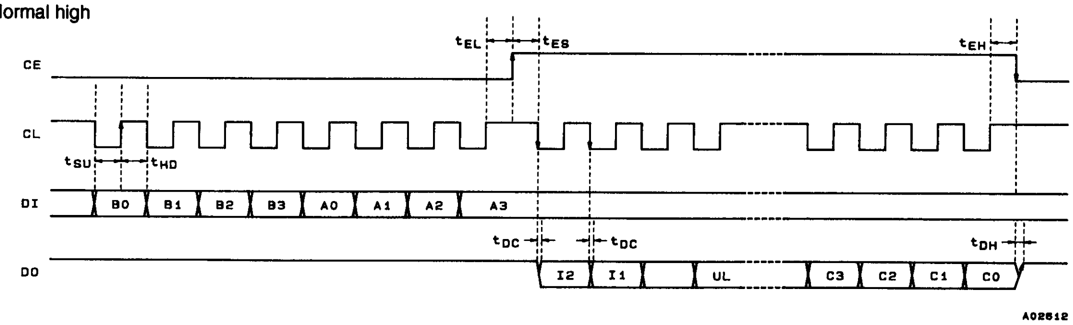


② CL: Normal low

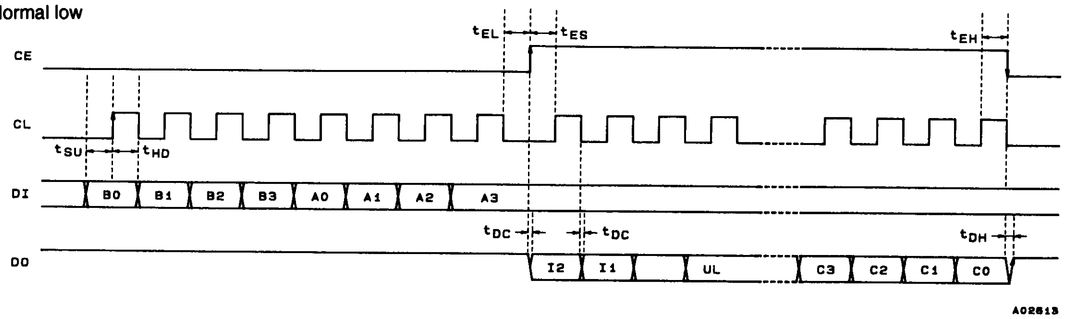


6. Serial Data Output (OUT) t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} ≥ 0.75 μs, t_{DC}, t_{DH} < 0.35 μs

① CL: Normal high

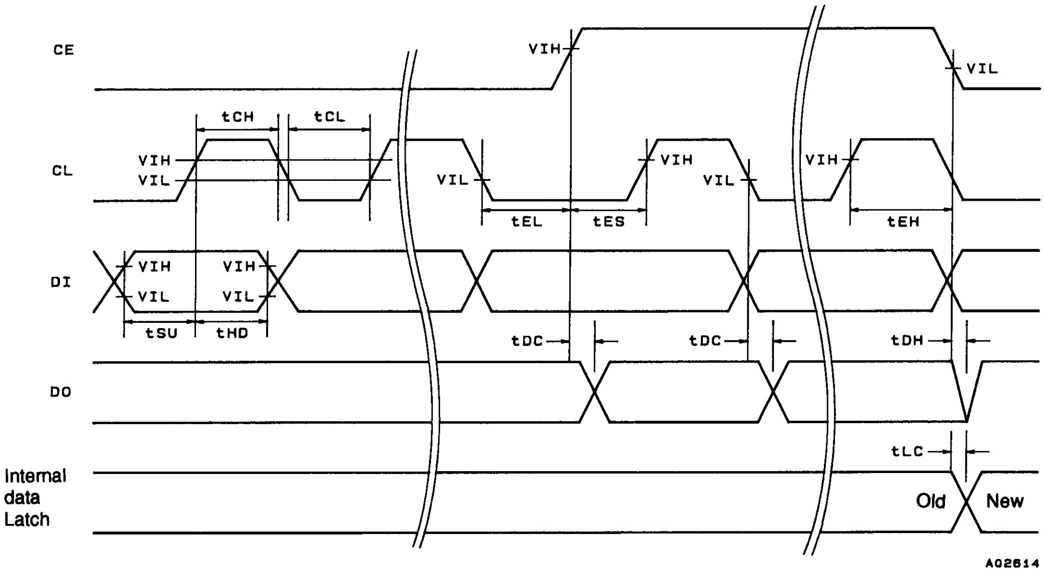


② CL: Normal low

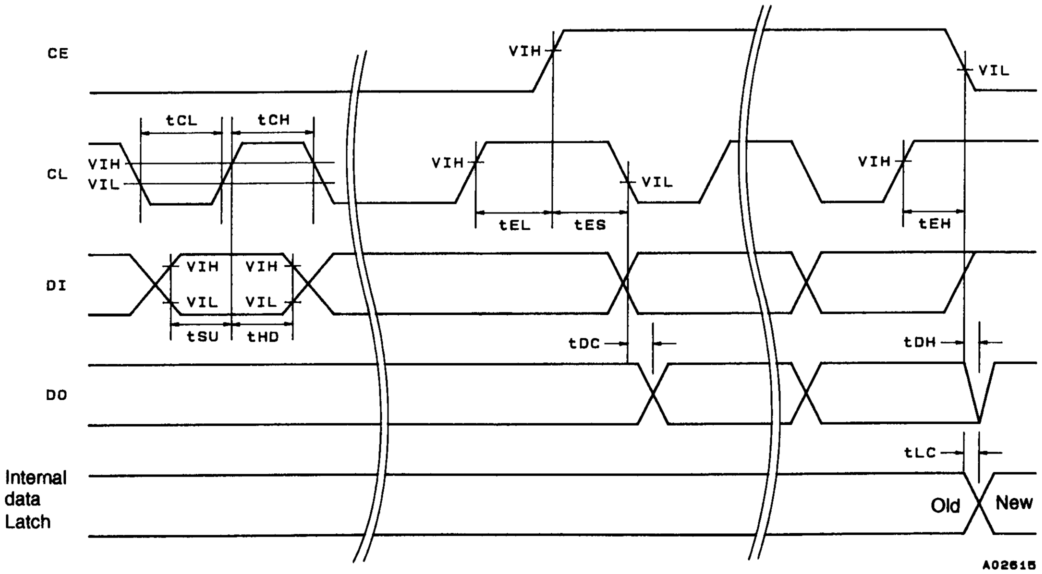


Note: Since the DO pin is an n-channel open-drain circuit, the time for the data to change (t_{DC} and t_{DH}) will differ depending on the value of the pull-up resistor and printed circuit, board capacitance.

7. Serial Data Timing



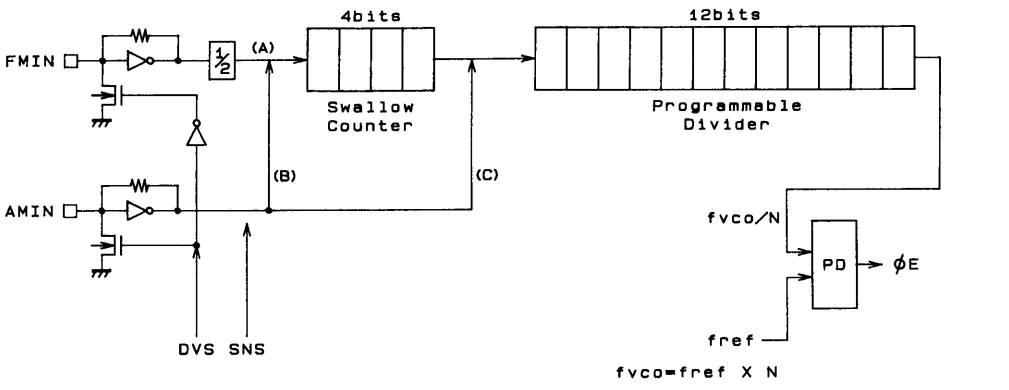
When stopped with CL low



When stopped with CL high

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Data setup time	t_{SU}	DI, CL		0.75			µs
Data hold time	t_{HD}	DI, CL		0.75			µs
Clock low-level time	t_{CL}	CL		0.75			µs
Clock high-level time	t_{CH}	CL		0.75			µs
CE wait time	t_{EL}	CE, CL		0.75			µs
CE setup time	t_{ES}	CE, CL		0.75			µs
CE hold time	t_{EH}	CE, CL		0.75			µs
Data latch change time	t_{LC}					0.75	µs
Data output time	t_{DC}	DO, CL	Differs depending on the value of the pull-up resistor and the printed circuit board capacitances.			0.35	µs
	t_{DH}	DO, CE					

Programmable Divider Structure



A02616

	DVS	SNS	Input pin	Set divisor	Actual divisor: N	Input frequency range (MHz)
A	1	*	FMIN	272 to 65535	Twice the set value	10 to 130
B	0	1	AMIN	272 to 65535	The set value	2 to 40
C	0	0	AMIN	4 to 4095	The set value	0.5 to 10

Note: * Don't care.

1. Programmable Divider Calculation Examples
   - FM, 50 kHz steps (DVS = 1, SNS = *, FMIN selected)
     FM RF = 80.0 MHz (IF = –10.7 MHz)
     FM VCO = 69.3 MHz
     PLL fref = 25 kHz (R0 to R1 = 1, R2 to R3 = 0)
     69.3 MHz (FM VCO) ÷ 25 kHz (fref) ÷ 2 (FMIN: divide-by-two prescaler) = 1386 → 056A (HEX)

A				6				5				0											
0	1	0	1	0	1	1	0	1	0	1	0	0	0	0	0	*	1			1	1	0	0
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A05793

   - SW, 5 kHz steps (DVS = 0, SNS = 1, AMIN high speed side selected)
     SW RF = 21.75 MHz (IF = +450 kHz)
     SW VCO = 22.20 MHz
     PLL fref = 5 kHz (R0 = R2 = 0, R1 = R3 = 1)
     22.2 MHz (SW VCO) ÷ 5 kHz (fref) = 4440 → 1158 (HEX)

8				5				1				1											
0	0	0	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0			0	1	0	1
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A02618

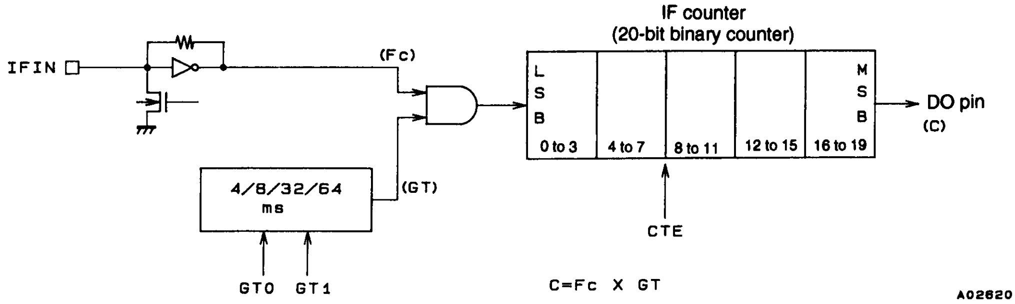
   - MW, 10 kHz steps (DVS = 0, SNS = 0, AMIN low-speed side selected)
     MW RF = 1000 kHz (IF = +450 kHz)
     MW VCO = 1450 kHz
     PLL fref = 10 kHz (R0 to R2 = 0, R3 = 1)
     1450 kHz (MW VCO) ÷ 10 kHz (fref) = 145 → 091 (HEX)

				1				9				0											
*	*	*	*	1	0	0	0	1	0	0	1	0	0	0	0	0	0			0	0	0	1
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A02619

IF Counter Structure

The LC72133 IF counter is a 20-bit binary counter. The result, i.e., the counter's MSB, can be read serially from the DO pin.



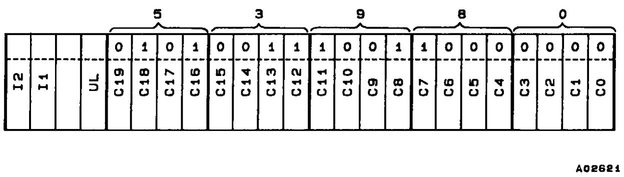
GT1	GT0	Measurement time	
		Measurement period (GT) (ms)	Wait time (twu) (ms)
0	0	4	3 to 4
0	1	8	3 to 4
1	0	32	7 to 8
1	1	64	7 to 8

The IF frequency (Fc) is measured by determining how many pulses were input to an IF counter in a specified measurement period, GT.

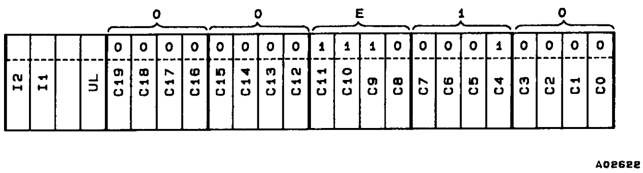
$Fc = \dfrac{C}{GT}$ (C = Fc $\times$ GT) C: Count value (number of pulses)

1. IF Counter Frequency Calculation Examples

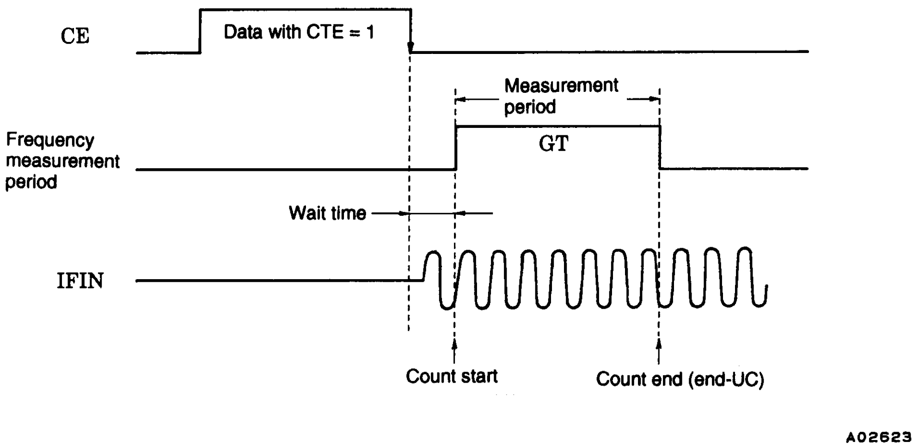
   • When the measurement period (GT) is 32 ms, the count (C) is 53980 hexadecimal (342400 decimal):
   IF frequency (Fc) = 342400 ÷ 32 ms = 10.7 MHz



   • When the measurement period (GT) is 8 ms, the count (C) is E10 hexadecimal (3600 decimal):
   IF frequency (Fc) = 3600 ÷ 8 ms = 450 kHz



2. IF Counter Operation



Before starting the IF count, the IF counter must be reset in advance by setting CTE in the serial data to 0.

The IF count is started by changing the CTE bit in the serial data from 0 to 1. The serial data is latched by the LC72133 when the CE pin is dropped from high to low. The IF signal must be supplied to the IFIN pin in the period between the point the CE pin goes low and the end of the wait time at the latest. Next, the value of the IF counter at the end of the measurement period must be read out during the period that CTE is 1. This is because the IF counter is reset when CTE is set to 0.

Note: When operating the IF counter, the control microprocessor must first check the state of the IF-IC SD (station detect) signal and only after determining that the SD signal is present turn on IF buffer output and execute an IF count operation. Autosearch techniques that use only the IF counter are not recommended, since it is possible for IF buffer leakage output to cause incorrect stops at points where there is no station.

IFIN minimum input sensitivity standard

f (MHz)

IFS	0.4 ≤ f < 0.5	0.5 ≤ f < 8	8 ≤ f ≤ 12
1: Normal mode	70 mVrms (0.5 to 5 mVrms)	70 mVrms	70 mVrms (2 to 10 mVrms)
0: Degradation mode	100 mVrms (10 to 15 mVrms)	100 mVrms	100 mVrms (30 to 50 mVrms)

Note: Values in parentheses are actual performance values presented as reference data.

Unlock Detection Timing

1. Unlock Detection Determination Timing

Unlocked state detection is performed in the reference frequency (fref) period (interval). Therefore, in principle, unlock determination requires a time longer than the period of the reference frequency. However, immediately after changing the divisor N (frequency) unlock detection must be performed after waiting at least two periods of the reference frequency.

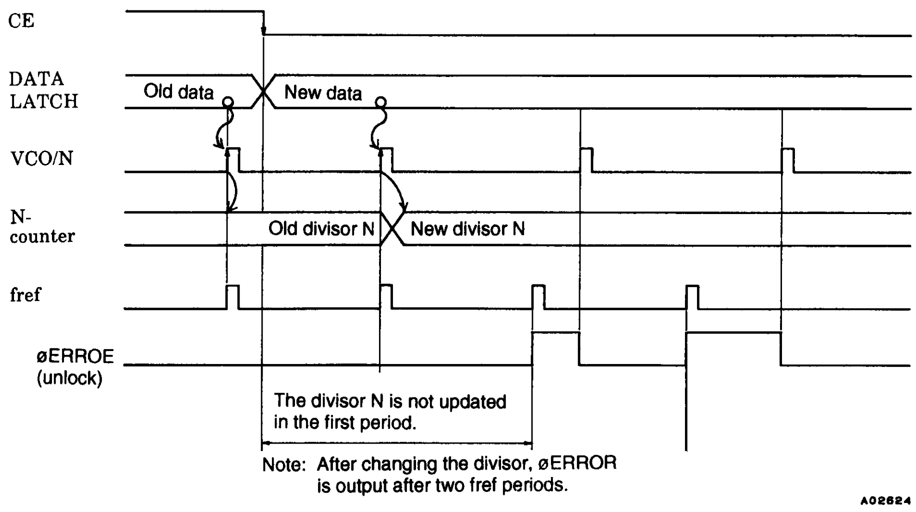


Figure 1 Unlocked State Detection Timing

For example, if fref is 1 kHz, i.e., the period is 1 ms, after changing the divisor N, the system must wait at least 2 ms before checking for the unlocked state.

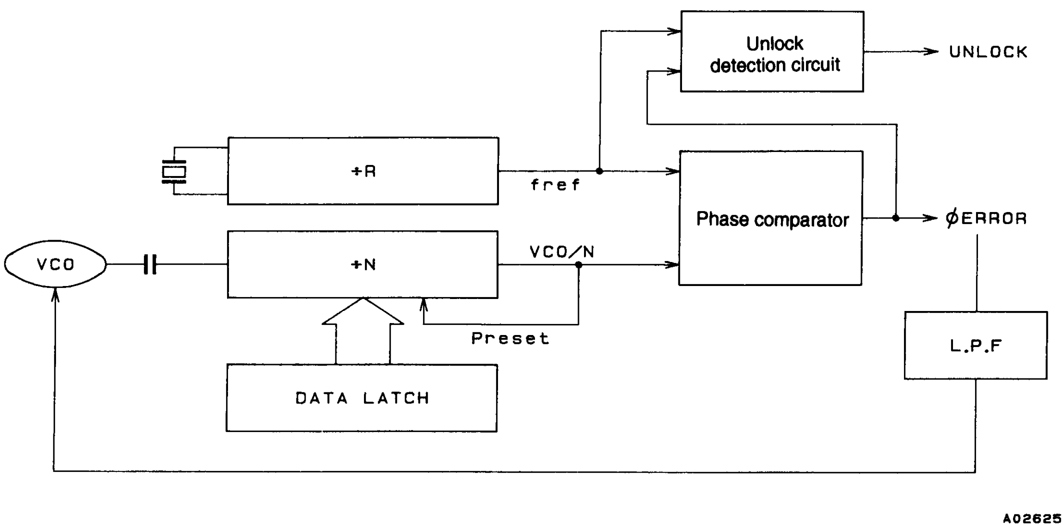


Figure 2 Circuit Structure

2. Unlock Detection Software

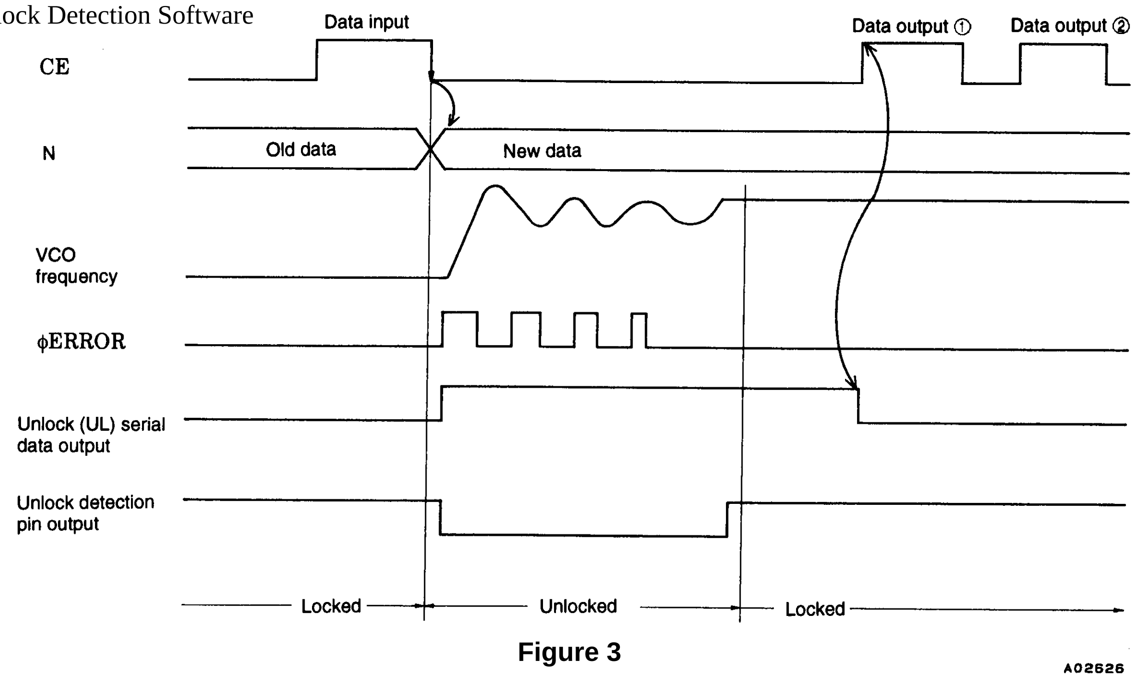
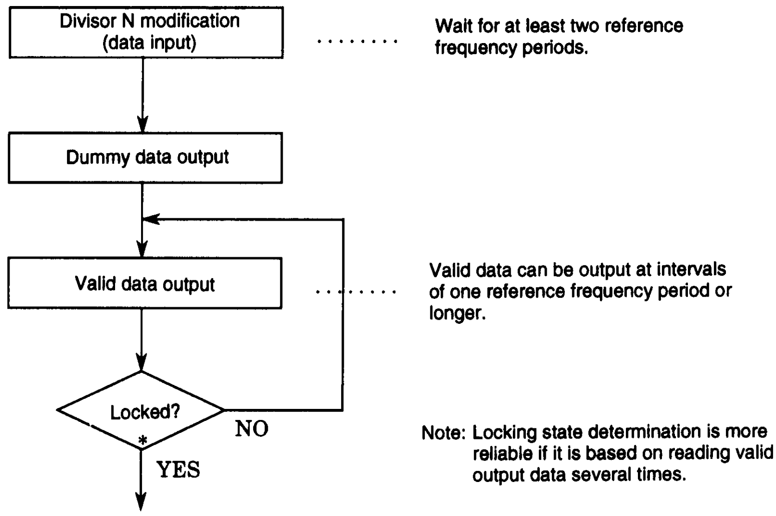


Figure 3

3. Unlocked State Data Output Using Serial Data Output

In the LC72133, once an unlocked state occurs, the unlocked state serial data (UL) will not be reset until a data input (or output) operation is performed. At the data output ① point in Figure 3, although the VCO frequency has stabilized (locked), since no data output has been performed since the divisor N was changed the unlocked state data remains in the unlocked state. As a result, even though the frequency has stabilized (locked), the system remains (from the standpoint of the data) in the unlocked state.
Therefore, the unlocked state data acquired at data output ①, which occurs immediately after the divisor N was changed, should be treated as a dummy data output and ignored. The second data output (data output ②) and following outputs are valid data.



Locked State Determination Flowchart

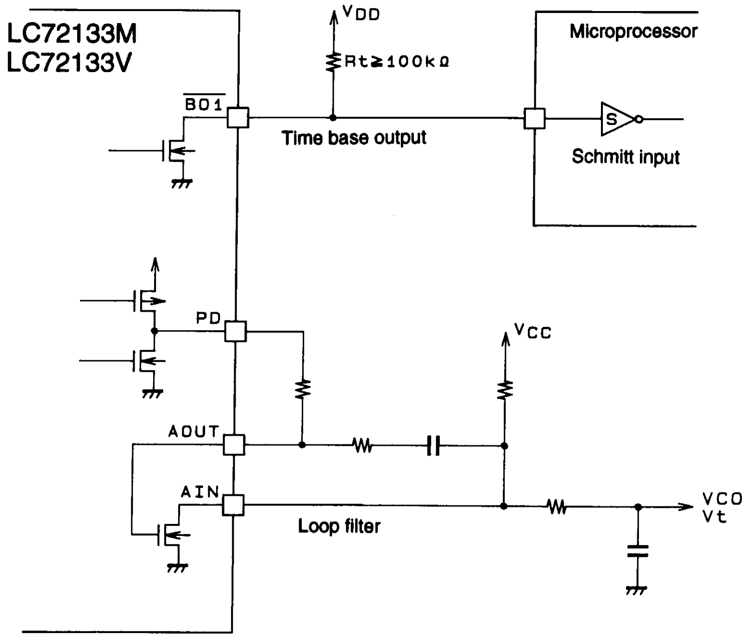
4. Directly Outputting Unlocked State Data from the DO Pin (Set by the DO pin control data)

Since the locking state (high = locked, low = unlocked) is output directly from the DO pin, the dummy data processing described in section 3 above is not required. After changing the divisor N, the locking state can be checked after waiting at least two reference frequency periods.

Clock Time Base Usage Notes

The pull-up resistor used on the clock time base output pin ($\overline{BO1}$) should be at least 100 kΩ. Also, to prevent chattering we recommend using a Schmitt input at the controller (microprocessor) that receives this signal.

This is to prevent degrading the VCO C/N characteristics when a loop filter is formed using the built-in low-pass filter transistor. Since the clock time base output pin and the low-pass filter have a common ground internal to the IC, it is necessary to minimize the time base output pin current fluctuations and to suppress their influence on the low-pass filter.



Other Items

1. Notes on the Phase Comparator Dead Zone

DZ1	DZ0	Dead zone mode	Charge pump	Dead zone
0	0	DZA	ON/ON	– –0 s
0	1	DZB	ON/ON	–0 s
1	0	DZC	OFF/OFF	+0 s
1	1	DZD	OFF/OFF	+ +0 s

Since correction pulses are output from the charge pump even if the PLL is locked when the charge pump is in the ON/ON state, the loop can easily become unstable. This point requires special care when designing application circuits.

The following problems may occur in the ON/ON state.

- Side band generation due to reference frequency leakage
- Side band generation due to both the correction pulse envelope and low frequency leakage

Schemes in which a dead zone is present (OFF/OFF) have good loop stability, but have the problem that acquiring a high C/N ratio can be difficult. On the other hand, although it is easy to acquire a high C/N ratio with schemes in which there is no dead zone, it is difficult to achieve high loop stability. Therefore, it can be effective to select DZA or DZB, which have no dead zone, in applications which require an FM S/N ratio in excess of 90 to 100 dB, or in which an increased AM stereo pilot margin is desired. On the other hand, we recommend selecting DZC or DZD, which provide a dead zone, for applications which do not require such a high FM signal-to-noise ratio and in which either AM stereo is not used or an adequate AM stereo pilot margin can be achieved.

Dead Zone

The phase comparator compares fp to a reference frequency (fr) as shown in Figure 4. Although the characteristics of this circuit (see Figure 5) are such that the output voltage is proportional to the phase difference ø (line A), a region (the dead zone) in which it is not possible to compare small phase differences occurs in actual ICs due to internal circuit delays and other factors (line B). A dead zone as small as possible is desirable for products that must provide a high S/N ratio.

However, since a larger dead zone makes this circuit easier to use, a larger dead zone is appropriate for popularly-priced products. This is because it is possible for RF signals to leak from the mixer to the VCO and modulate the VCO in popularly-priced products in the presence of strong RF inputs. When the dead zone is narrow, the circuit outputs correction pulses and this output can further modulate the VCO and generate beat frequencies with the RF signal.

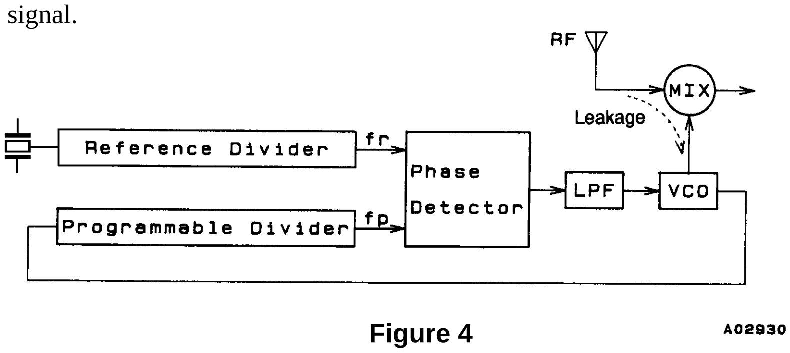


Figure 4

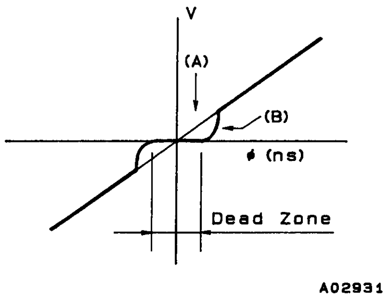


Figure 5

2. Notes on the FMIN, AMIN, and IFIN Pins

   Coupling capacitors must be placed as close as possible to their respective pin. A capacitance of about 100 pF is desirable. In particular, if a capacitance of 1000 pF or over is used for the IF pin, the time to reach the bias level will increase and incorrect counting may occur due to the relationship with the wait time.

3. Notes on IF Counting → SD must be used in conjunction with the IF counting time

   When using IF counting, always implement IF counting by having the microprocessor determine the presence of the IF-IC SD (station detect) signal and turn on the IF counter buffer only if the SD signal is present. Schemes in which auto-searches are performed with only IF counting are not recommended, since they can stop at points where there is no signal due to leakage output from the IF counter buffer.

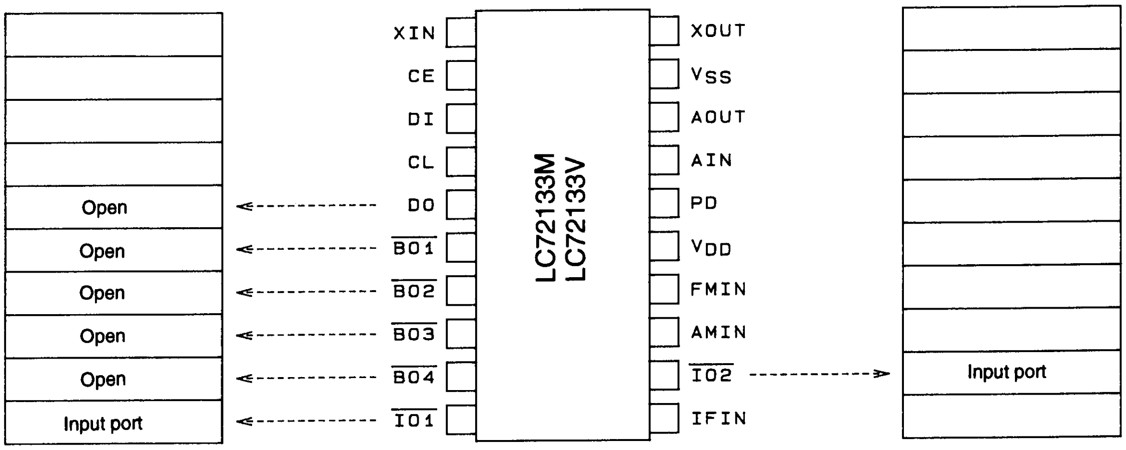
4. DO Pin Usage Techniques

   In addition to data output mode times, the DO pin can also be used to check for IF counter count completion and for unlock detection output. Also, an input pin state can be output unchanged through the DO pin and input to the controller.

5. Power Supply Pins

   A capacitor of at least 2000 pF must be inserted between the power supply V_{DD} and V_{SS} pins for noise exclusion. This capacitor must be placed as close as possible to the V_{DD} and V_{SS} pins.

Pin States After the Power ON Reset



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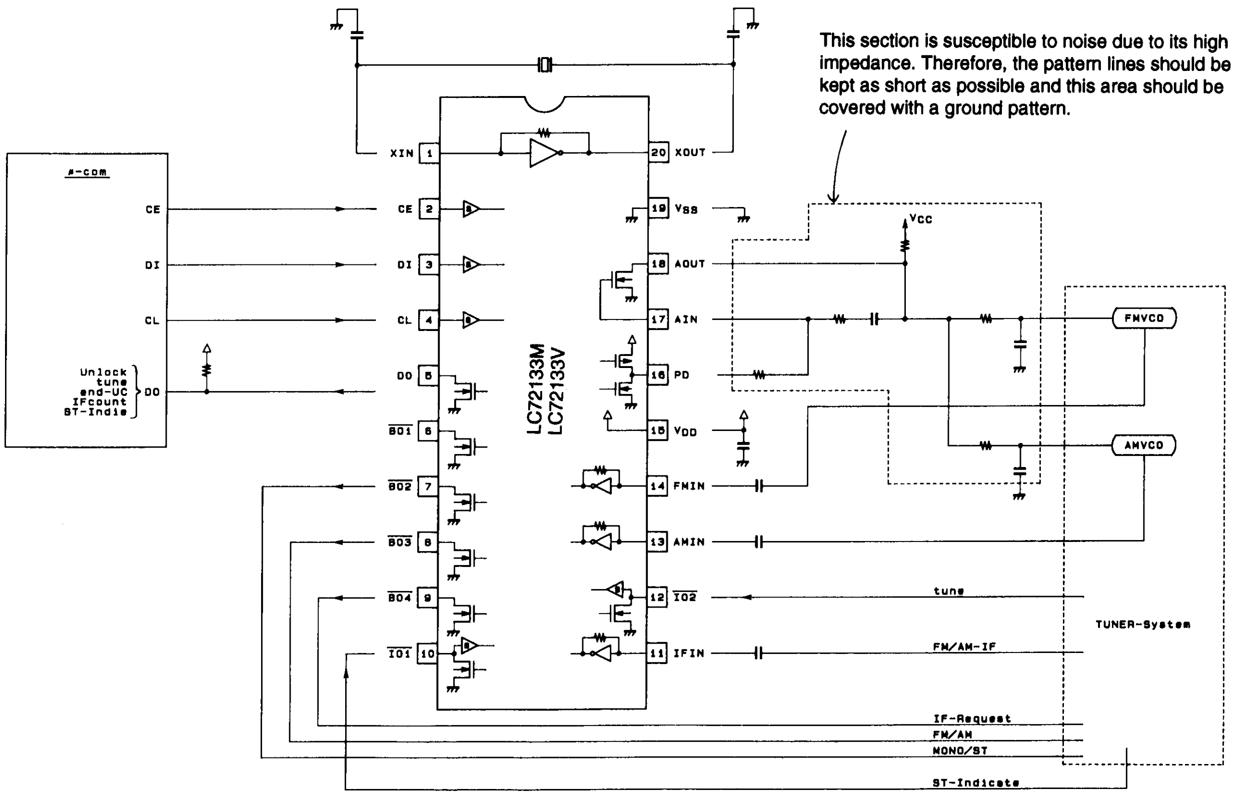
Application System Example



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This catalog provides information as of February, 1997. Specifications and information herein are subject to change without notice.