



Integrated Device Technology, Inc.

**BiCMOS StaticRAM**  
**240K (16K x 15-BIT)**  
**CACHE-TAG RAM**  
**For PowerPC™ and RISC Processors**

**IDT71216**

**FEATURES:**

- 16K x 15 Configuration
  - 12 TAG Bits
  - 3 Separate I/O Status Bits (Valid, Dirty, Write Through)
- Match output uses Valid bit to qualify MATCH output
- High-Speed Address-to-Match comparison times
  - 8/9/10/12ns over commercial temperature range
- $\overline{\text{TA}}$  circuitry included inside the Cache-Tag for highest speed operation
- Asynchronous Read/Match operation with Synchronous Write and Reset operation
- Separate  $\overline{\text{WE}}$  for the TAG bits and the Status bits
- Separate  $\overline{\text{OE}}$  for the TAG bits, the Status bits, and  $\overline{\text{TA}}$
- Synchronous  $\overline{\text{RESET}}$  pin for invalidation of all Tag entries
- Dual Chip selects for easy depth expansion with no performance degradation
- I/O pins both 5V TTL and 3.3V LVTTTL compatible with VCCQ pins
- $\overline{\text{PWRDN}}$  pin to place device in low-power mode
- Packaged in a 80-pin Thin Plastic Quad Flat Pack (TQFP)

**DESCRIPTION:**

The IDT71216 is a 245,760-bit Cache Tag StaticRAM, organized 16K x 15 and designed to support PowerPC and other RISC processors at bus speeds up to 66MHz. There are twelve common I/O TAG bits, with the remaining three bits used as status bits. A 12-bit comparator is on-chip to allow fast comparison of the twelve stored TAG bits and the current Tag input data. An active HIGH MATCH output is generated when these two groups of data are the same for a given address.

This high-speed MATCH signal, with  $t_{\text{ADM}}$  as fast as 8ns, provides the fastest possible enabling of secondary cache accesses.

The three separate I/O status bits (VLD, DTY, and WT) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC LOW, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given Tag data. SFUNC HIGH releases the defined internal status bit usage and control, allowing the user to configure the status bit information to fit his system needs. A synchronous  $\overline{\text{RESET}}$  pin, when held LOW at a rising clock edge, will reset all status bits in the array for easy invalidation of all Tag addresses.

The IDT71216 also provides the option for Transfer Acknowledge ( $\overline{\text{TA}}$ ) generation within the cache tag itself, based upon MATCH, VLD bit, WT bit, and external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and Read operations are both asynchronous in order to provide the fastest access times possible, while Write operations are synchronous for ease of system timing.

The IDT71216 uses a 5V power supply on Vcc, with separate VCCQ pins provided for the outputs to offer compliance with both 5.0V TTL and 3.3V LVTTTL Logic levels. The  $\overline{\text{PWRDN}}$  pin offers a low-power standby mode to reduce power consumption by 90%, providing significant system power savings.

The IDT71216 is fabricated using IDT's high-performance, high-reliability BiCMOS technology and is offered in a space-saving 80-pin Thin Plastic Quad Flat Pack (TQFP) package.

**PIN DESCRIPTIONS**

|                                      |                                  |       |
|--------------------------------------|----------------------------------|-------|
| A0 – A13                             | Address Inputs                   | Input |
| $\overline{\text{CS1}}, \text{CS2}$  | Chip Selects                     | Input |
| $\overline{\text{WET}}$              | Write Enable - Tag Bits          | Input |
| $\overline{\text{WES}}$              | Write Enable - Status Bits       | Input |
| $\overline{\text{OET}}$              | Output Enable - Tag Bits         | Input |
| $\overline{\text{OES}}$              | Output Enable - Status Bits      | Input |
| $\overline{\text{RESET}}$            | Status Bit Reset                 | Input |
| $\overline{\text{PWRDN}}$            | Powerdown Mode Control Pin       | Input |
| SFUNC                                | Status Bit Function Control Pin  | Input |
| TT1                                  | Read/Write Input from Processor  | Input |
| VLD <sub>IN</sub> / S1 <sub>IN</sub> | Valid Bit / S1 Bit Input         | Input |
| DTY <sub>IN</sub> / S2 <sub>IN</sub> | Dirty Bit / S2 Bit Input         | Input |
| WT <sub>IN</sub> / S3 <sub>IN</sub>  | Write Through Bit / S3 Bit Input | Input |

|  |   |        |
|--|---|--------|
| CLK                                    | System Clock                            | Input  |
| TAH                                    | $\overline{\text{TA}}$ Force High       | Input  |
| $\overline{\text{TAOE}}$               | $\overline{\text{TA}}$ Output Enable    | Input  |
| $\overline{\text{TAIN}}$               | Additional $\overline{\text{TA}}$ Input | Input  |
| $\overline{\text{TA}}$                 | Transfer Acknowledge                    | Output |
| TAG0 – TAG11                           | Tag Data Input/Outputs                  | I/O    |
| VLD <sub>OUT</sub> / S1 <sub>OUT</sub> | Valid Bit / S1 Bit Output               | Output |
| DTY <sub>OUT</sub> / S2 <sub>OUT</sub> | Dirty Bit / S2 Bit Output               | Output |
| WT <sub>OUT</sub> / S3 <sub>OUT</sub>  | Write Through Bit / S3 Bit Output       | Output |
| MATCH                                  | Match                                   | Output |
| VCC                                    | +5V Power                               | Pwr    |
| VCCQ                                   | Output Buffer Power                     | QPwr   |
| VSS                                    | Ground                                  | Gnd    |

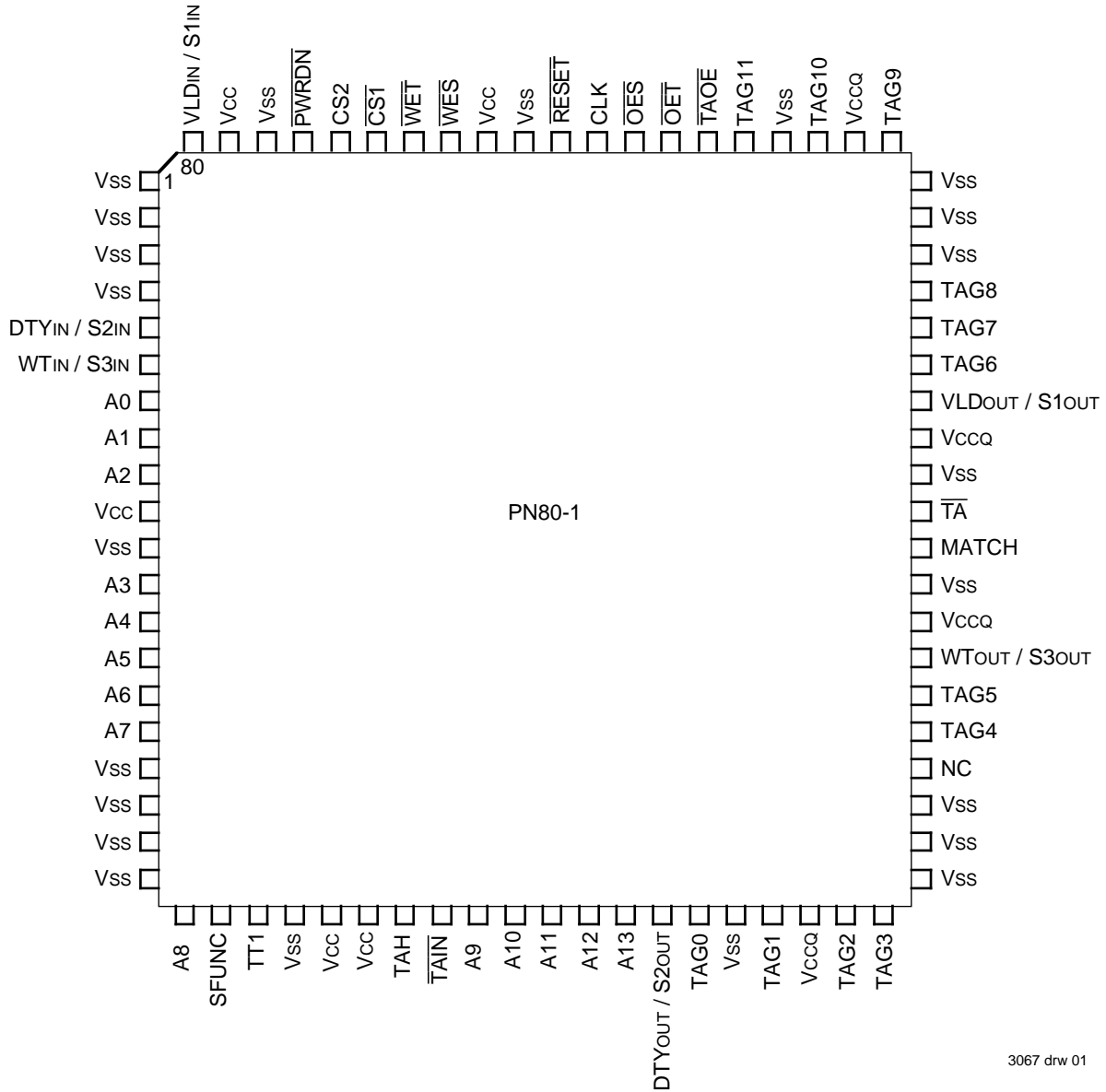
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3067 tbl 01

**COMMERCIAL TEMPERATURE RANGE**

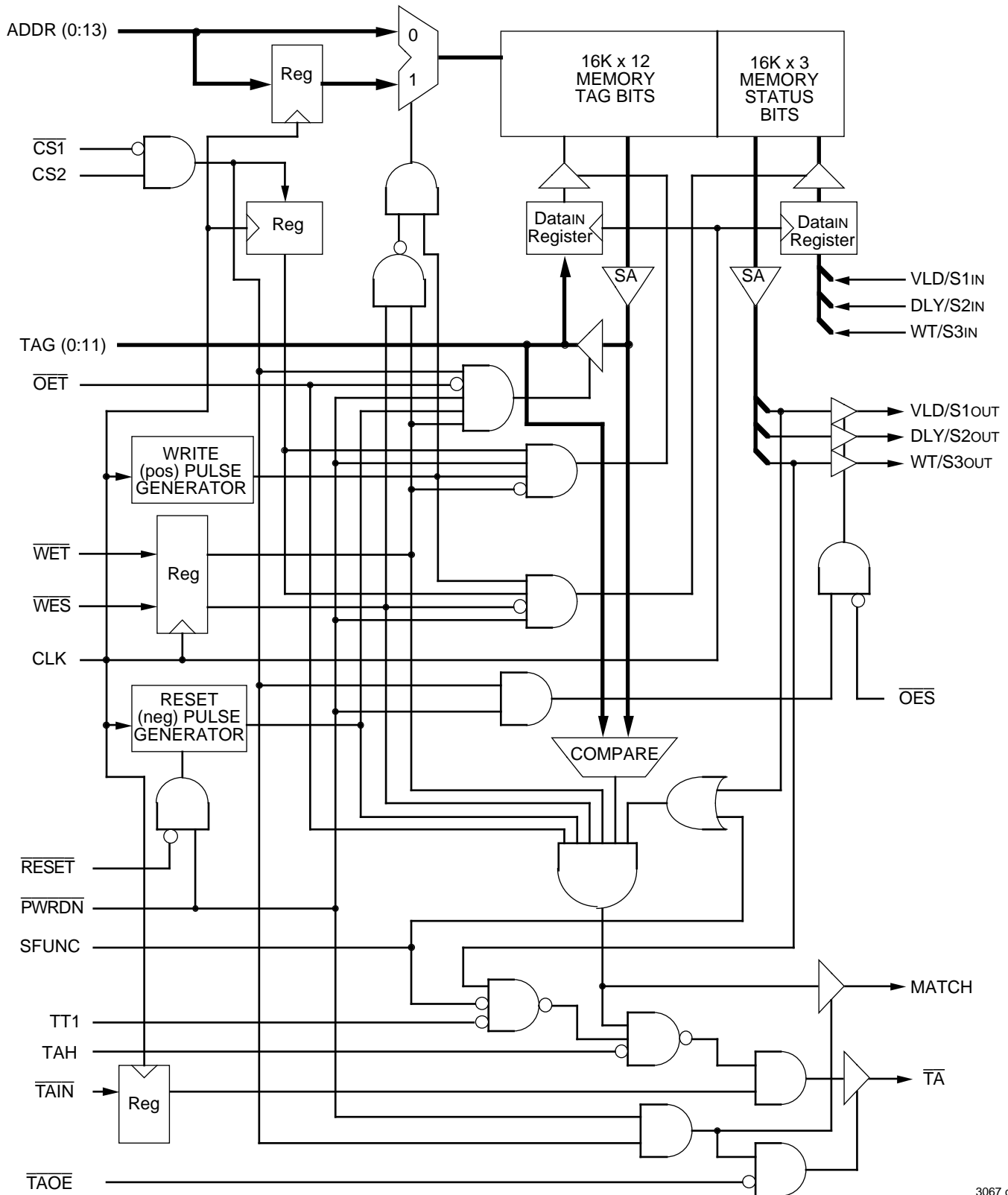
**AUGUST 1996**

**PIN CONFIGURATION**



**TQFP  
 TOP VIEW**

FUNCTIONAL BLOCK DIAGRAM



3067 drw 02

## TRUTH TABLES

### CHIP SELECT, RESET, AND POWER-DOWN FUNCTIONS<sup>(1, 2)</sup>

| CS1 | CS2 | RESET | PWRDN | CLK | WET | WES | TAOE | TAG | VLDout | DTYout | WTout | MATCH | TA | OPERATION | POWER |
|-----|-----|-------|-------|-----|-----|-----|------|-----|--------|--------|-------|-------|----|-----------|-------|
|-----|-----|-------|-------|-----|-----|-----|------|-----|--------|--------|-------|-------|----|-----------|-------|

#### CHIP SELECT FUNCTION

|   |   |   |   |   |   |   |   |      |      |      |      |      |      |            |        |
|---|---|---|---|---|---|---|---|------|------|------|------|------|------|------------|--------|
| H | X | X | H | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Deselected | Active |
| X | L | X | H | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Deselected | Active |
| L | H | X | H | X | X | X | X | -    | -    | -    | -    | -    | -    | Selected   | Active |

#### RESET FUNCTION

|   |   |   |   |   |   |   |   |      |                  |                  |                  |                  |      |              |        |
|---|---|---|---|---|---|---|---|------|------------------|------------------|------------------|------------------|------|--------------|--------|
| L | H | L | H | ↑ | H | H | L | Hi-Z | L <sup>(3)</sup> | L <sup>(3)</sup> | L <sup>(3)</sup> | L <sup>(3)</sup> | H    | Reset Status | Active |
| L | H | L | H | ↑ | H | H | H | Hi-Z | L <sup>(3)</sup> | L <sup>(3)</sup> | L <sup>(3)</sup> | L <sup>(3)</sup> | Hi-Z | Reset Status | Active |
| H | X | L | H | ↑ | H | H | X | Hi-Z | Hi-Z             | Hi-Z             | Hi-Z             | Hi-Z             | Hi-Z | Reset Status | Active |
| X | L | L | H | ↑ | H | H | X | Hi-Z | Hi-Z             | Hi-Z             | Hi-Z             | Hi-Z             | Hi-Z | Reset Status | Active |
| X | X | L | H | ↑ | L | X | X | -    | -                | -                | -                | -                | -    | Not Allowed  | -      |
| X | X | L | H | ↑ | X | L | X | -    | -                | -                | -                | -                | -    | Not Allowed  | -      |

#### POWER-DOWN FUNCTION

|   |   |   |   |   |   |   |   |      |      |      |      |      |      |            |         |
|---|---|---|---|---|---|---|---|------|------|------|------|------|------|------------|---------|
| X | X | X | L | X | H | H | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Power-down | Standby |
|---|---|---|---|---|---|---|---|------|------|------|------|------|------|------------|---------|

#### NOTES:

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = don't care, "-" = unrelated.
- $\overline{OET}$ ,  $\overline{OES}$ , TT1, TAH,  $\overline{TAIN}$  and SFUNC are "X" for this table.
- OES is LOW.

3067 tbl 02

### READ AND WRITE FUNCTIONS<sup>(1, 2)</sup>

| $\overline{OET}$ | $\overline{OES}$ | WET | WES | CLK | TT1 | TAG | VLDin | DTYin | WTin | VLDout | DTYout | WTout | MATCH | OPERATION |
|------------------|------------------|-----|-----|-----|-----|-----|-------|-------|------|--------|--------|-------|-------|-----------|
|------------------|------------------|-----|-----|-----|-----|-----|-------|-------|------|--------|--------|-------|-------|-----------|

#### READ FUNCTION

|   |   |   |   |   |   |      |   |   |   |      |      |      |      |                  |
|---|---|---|---|---|---|------|---|---|---|------|------|------|------|------------------|
| L | X | H | X | X | X | DOUT | - | - | - | -    | -    | -    | DOUT | Read TAG I/O     |
| X | L | X | X | X | X | -    | - | - | - | DOUT | DOUT | DOUT | DOUT | Read Status Bits |
| H | X | X | X | X | X | Hi-Z | - | - | - | -    | -    | -    | DOUT | TAG I/O Disable  |
| X | H | X | X | X | X | -    | - | - | - | Hi-Z | Hi-Z | Hi-Z | DOUT | Status Disabled  |

#### WRITE FUNCTION

|   |   |   |   |   |   |     |     |     |     |                     |                     |                     |   |                   |
|---|---|---|---|---|---|-----|-----|-----|-----|---------------------|---------------------|---------------------|---|-------------------|
| H | X | L | X | ↑ | X | DIN | -   | -   | -   | DOUT                | DOUT                | DOUT                | L | Write TAG I/O     |
| L | X | L | X | ↑ | X | -   | -   | -   | -   | -                   | -                   | -                   | - | Not Allowed       |
| X | L | X | L | ↑ | X | -   | DIN | DIN | DIN | DOUT <sup>(3)</sup> | DOUT <sup>(3)</sup> | DOUT <sup>(3)</sup> | L | Write Status Bits |
| X | H | X | L | ↑ | X | -   | DIN | DIN | DIN | Hi-Z                | Hi-Z                | Hi-Z                | L | Write Status Bits |

#### NOTES:

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = don't care, "-" = unrelated.
- This table applies when CS1 is LOW and CS2, RESET, and PWRDN are HIGH.  $\overline{TAOE}$ , TAH,  $\overline{TAIN}$  and SFUNC are "X" for this table.
- DOUT in this case is the same as DIN; that is, the input data is written through to the outputs during the write operation.

3067 tbl 03

## TRUTH TABLES (CONT.)

### MATCH FUNCTION<sup>(1, 2, 3)</sup>

| CS1 | CS2 | SFUNC | OET | WET | WES | TAG   | VLD <sup>(4)</sup> | DTY <sup>(4)</sup> | WT <sup>(4)</sup> | MATCH | OPERATION                            |
|-----|-----|-------|-----|-----|-----|-------|--------------------|--------------------|-------------------|-------|--------------------------------------|
| H   | X   | X     | X   | X   | X   | Hi-Z  | –                  | –                  | –                 | Hi-Z  | Deselected                           |
| X   | L   | X     | X   | X   | X   | Hi-Z  | –                  | –                  | –                 | Hi-Z  | Deselected                           |
| L   | H   | X     | X   | X   | X   | –     | –                  | –                  | –                 | DOUT  | Selected                             |
| L   | H   | X     | L   | H   | X   | DOUT  | –                  | –                  | –                 | L     | Read Tag I/O                         |
| L   | H   | X     | H   | L   | X   | DIN   | –                  | –                  | –                 | L     | Write Tag I/O                        |
| L   | H   | X     | X   | X   | L   | –     | DIN                | DIN                | DIN               | L     | Write Status Bits                    |
| L   | H   | L     | H   | H   | H   | TAGIN | L                  | –                  | –                 | L     | Invalid Data - Dedicated Status Bits |
| L   | H   | L     | H   | H   | H   | TAGIN | H                  | –                  | –                 | M     | Match - Dedicated Status Bits        |
| L   | H   | H     | H   | H   | H   | TAGIN | X                  | –                  | –                 | M     | Match - Generic Status Bits          |

**NOTES:**

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = don't care, "–" = unrelated.
- M = HIGH if TAGIN equals the memory contents at that address; M = LOW if TAGIN does not equal the memory contents at that address.
- PWRDN and RESET are HIGH for this table. TT1, TAH, TAOE, TAIN, OES, and CLK are "X".
- This column represents the stored memory cell data for the given Status bit at the selected address.

3067 tbl 04

### TĀ FUNCTION<sup>(1, 2, 3, 5)</sup>

| TAOE | TAIN <sup>(6)</sup> | OET | WET | WES | TAH | TT1 | SFUNC | VLD <sup>(4)</sup> | DTY <sup>(4)</sup> | WT <sup>(4)</sup> | TAG   | MATCH | TĀ   | OPERATION                        |
|------|---------------------|-----|-----|-----|-----|-----|-------|--------------------|--------------------|-------------------|-------|-------|------|----------------------------------|
| H    | X                   | X   | X   | X   | X   | X   | X     | X                  | –                  | X                 | –     | –     | Hi-Z | TĀ Disabled                      |
| L    | L                   | X   | X   | X   | X   | X   | X     | X                  | –                  | X                 | –     | X     | L    | External TĀ Input <sup>(7)</sup> |
| L    | H                   | L   | X   | X   | X   | X   | X     | X                  | –                  | X                 | DOUT  | L     | H    | Read TAG                         |
| L    | H                   | X   | L   | X   | X   | X   | X     | X                  | –                  | X                 | DIN   | L     | H    | Write TAG                        |
| L    | H                   | X   | X   | L   | X   | X   | X     | DIN                | DIN                | DIN               | –     | L     | H    | Write Status                     |
| L    | H                   | X   | X   | X   | H   | X   | X     | X                  | –                  | X                 | –     | X     | H    | Force TĀ HIGH                    |
| L    | H                   | X   | X   | X   | X   | X   | L     | L                  | –                  | X                 | –     | L     | H    | Invalid TAG                      |
| L    | H                   | X   | X   | X   | X   | L   | L     | X                  | –                  | H                 | –     | X     | H    | Write Through                    |
| L    | H                   | H   | H   | H   | L   | X   | L     | H                  | –                  | L                 | TAGIN | M     | M̄   | Compare                          |
| L    | H                   | H   | H   | H   | L   | H   | L     | H                  | –                  | X                 | TAGIN | M     | M̄   | Compare                          |
| L    | H                   | H   | H   | H   | L   | X   | L     | H                  | –                  | X                 | TAGIN | M     | M̄   | Compare                          |
| L    | H                   | H   | H   | H   | L   | X   | H     | X                  | –                  | X                 | TAGIN | M     | M̄   | Compare                          |

**NOTES:**

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = don't care, "–" = unrelated.
- M = HIGH if TAGIN equals the memory contents at that address; M = LOW if TAGIN does not equal the memory contents at that address.
- PWRDN and RESET are HIGH for this table. CLK and OES are "X".
- This column represents the stored memory cell data for the given Status bit at the selected address.
- CS1 is LOW, CS2 is HIGH for this table.
- TAIN is a synchronous input; thus the inputs noted in the table must be applied during a rising CLK edge.
- TAIN will be a factor in determining the TĀ output in all cases except when TAH is HIGH and there is a valid MATCH. In that case, TĀ will be LOW(Valid).

3067 tbl 05

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol           | Parameter           | Min.                | Typ. | Max.                  | Unit |
|------------------|---------------------|---------------------|------|-----------------------|------|
| V <sub>CC</sub>  | Supply Voltage      | 4.75                | 5.0  | 5.25                  | V    |
| V <sub>CCQ</sub> | 5V Output Buffers   | 4.75                | 5.0  | 5.25                  | V    |
| V <sub>CCQ</sub> | 3.3V Output Buffers | 3.0                 | 3.3  | 3.6                   | V    |
| V <sub>SS</sub>  | Supply Ground       | 0                   | 0    | 0                     | V    |
| V <sub>IH</sub>  | Input High Voltage  | 2.2                 | 3.0  | V <sub>CC</sub> +0.3  | V    |
| V <sub>IHQ</sub> | I/O High Voltage    | 2.2                 | 3.0  | V <sub>CCQ</sub> +0.3 | V    |
| V <sub>IL</sub>  | Input Low Voltage   | -0.5 <sup>(1)</sup> | —    | 0.8                   | V    |

**NOTE:** 3067 tbl 06  
1. V<sub>IL</sub> (min.) = -1.5V for pulse width of less than 10ns, once per cycle.

## CAPACITANCE

(T<sub>A</sub> = +25°C, f = 1.0 MHz)

| Symbol           | Parameter <sup>(1)</sup>     | Condition             | Max. | Unit |
|------------------|------------------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance            | V <sub>IN</sub> = 0V  | 5    | pF   |
| C <sub>TAG</sub> | TAG Input/Output Capacitance | V <sub>I/O</sub> = 0V | 7    | pF   |
| C <sub>OUT</sub> | Output Capacitance           | V <sub>OUT</sub> = 0V | 7    | pF   |

**NOTE:** 3067 tbl 07  
1. This parameter is determined by device characterization but is not production tested.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol            | Rating                               | Value                       | Unit |
|-------------------|--------------------------------------|-----------------------------|------|
| V <sub>TERM</sub> | Terminal Voltage with Respect to GND | -0.5 to +7.0 <sup>(2)</sup> | V    |
| T <sub>A</sub>    | Operating Temperature                | -0 to +70                   | °C   |
| T <sub>BIAS</sub> | Temperature Under Bias               | -65 to +135                 | °C   |
| T <sub>STG</sub>  | Storage Temperature                  | -65 to +150                 | °C   |
| P <sub>T</sub>    | Power Dissipation                    | 1.7                         | W    |
| I <sub>OUT</sub>  | DC Output Current                    | 20                          | mA   |

**NOTES:** 3067 tbl 08  
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.  
2. V<sub>IN</sub> should not exceed V<sub>CC</sub>+0.5V. All pins should not exceed 7.0V. V<sub>CCQ</sub> should never exceed V<sub>CC</sub>, and V<sub>CC</sub> should never exceed V<sub>CCQ</sub> + 4.0V.

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(V<sub>CC</sub> = 5.0V ± 5%, V<sub>CCQ</sub> = 5.0V ± 5% OR 3.3V ± 0.3V)

| Symbol          | Parameter              | Test Condition   | Min. | Max. | Unit |
|-----------------|------------------------|--|------|------|------|
| I <sub>L</sub>  | Input Leakage Current  | V <sub>CC</sub> = Max., V <sub>IN</sub> = 0V to V <sub>CC</sub>  | —    | 5    | μA   |
| I <sub>O</sub>  | Output Leakage Current | $\overline{CS1} \geq V_{IH}$ , $CS2 \leq V_{IL}$ , $\overline{OE} \geq V_{IH}$ , V <sub>CC</sub> = Max.<br>V <sub>OUT</sub> = 0V to V <sub>CCQ</sub> , V <sub>CCQ</sub> = Max. | —    | 5    | μA   |
| V <sub>OL</sub> | Output Low Voltage     | I <sub>OL</sub> = 4mA, V <sub>CC</sub> = Min.  | —    | 0.4  | V    |
| V <sub>OH</sub> | Output High Voltage    | I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.   | 2.4  | —    | V    |

3067 tbl 09

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE<sup>(1, 2)</sup> (V<sub>CC</sub> = 5.0V ± 5%)

| Symbol           | Parameter                         | Test Condition   | 71216S8 |      | 71216S9 |      | 71216S10 |      | 71216S12 |      | Unit |
|------------------|-----------------------------------|--|---------|------|---------|------|----------|------|----------|------|------|
|                  |                                   |  | Com'l.  | Mil. | Com'l.  | Mil. | Com'l.   | Mil. | Com'l.   | Mil. |      |
| I <sub>CC</sub>  | Operating Power Supply Current    | $\overline{PWRDN} \geq V_{IH}$<br>Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(3)</sup>  | 330     | —    | 300     | —    | 290      | —    | 280      | —    | mA   |
| I <sub>SB</sub>  | Standby Power Supply Current      | $\overline{PWRDN} \leq V_{IL}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub><br>V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(3)</sup> | 30      | —    | 30      | —    | 30       | —    | 30       | —    | mA   |
| I <sub>SB1</sub> | Full Standby Power Supply Current | $\overline{PWRDN} \leq V_{IL}$ , V <sub>IN</sub> ≥ V <sub>HC</sub> or ≤ V <sub>LC</sub> <sup>(4)</sup><br>V <sub>CC</sub> = Max., f = 0 <sup>(3)</sup> | 25      | —    | 25      | —    | 25       | —    | 25       | —    | mA   |

**NOTES:** 3067 tbl 10  
1. All values are maximum guaranteed values.  
2.  $\overline{CS1} \leq V_{IL}$ , CS2 ≥ V<sub>IH</sub>.  
3. f<sub>MAX</sub> = 1/t<sub>CYC</sub> (all address inputs are cycling at f<sub>MAX</sub>). f = 0 means no address input lines are changing.  
4. V<sub>HC</sub> = V<sub>CC</sub> - 0.2V, V<sub>LC</sub> = 0.2V

## AC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ± 5%, V<sub>CCQ</sub> = 5.0V ± 5% OR 3.3V ± 0.3V, T<sub>A</sub> = 0 to 70°C)

| Symbol               | Parameter                                    | IDT71216S8 |      | IDT71216S9 |      | IDT71216S10 |      | IDT71216S12 |      | Unit |
|----------------------|--|------------|------|------------|------|-------------|------|-------------|------|------|
|                      |  | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.        | Max. |      |
| <b>Read Cycle</b>    |  |            |      |            |      |             |      |             |      |      |
| tAAT                 | Address Access Time Tag Bits                 | —          | 10   | —          | 11   | —           | 12   | —           | 14   | ns   |
| tACST                | Chip Select Access Time Tag Bits             | —          | 8    | —          | 9    | —           | 10   | —           | 12   | ns   |
| tCLZ <sup>(1)</sup>  | Chip Select to Tag and Status Bits in Low-Z  | 1          | —    | 1          | —    | 1           | —    | 1           | —    | ns   |
| tCHZ <sup>(1)</sup>  | Chip Select to Tag and Status Bits in High-Z | 1          | 5    | 1          | 6    | 1           | 6    | 1           | 7    | ns   |
| tOET                 | Output Enable to Tag Bits Valid              | —          | 5    | —          | 6    | —           | 6    | —           | 7    | ns   |
| tOTLZ <sup>(1)</sup> | Output Enable to Tag Bits in Low-Z           | 0          | —    | 0          | —    | 0           | —    | 0           | —    | ns   |
| tOTHZ <sup>(1)</sup> | Output Enable to Tag Bits in High-Z          | 1          | 5    | 1          | 6    | 1           | 6    | 1           | 7    | ns   |
| tTOH                 | Tag Bit Hold from Address Change             | 2          | —    | 2          | —    | 2           | —    | 2           | —    | ns   |
| tOES                 | Output Enable to Status Bits Valid           | —          | 5    | —          | 6    | —           | 6    | —           | 7    | ns   |
| tOSLZ <sup>(1)</sup> | Output Enable to Status Bits in Low-Z        | 0          | —    | 0          | —    | 0           | —    | 0           | —    | ns   |
| tOSHZ <sup>(1)</sup> | Output Enable to Status Bits in High-Z       | 1          | 5    | 1          | 6    | 1           | 6    | 1           | 7    | ns   |
| tAAS                 | Address Access Time Status Bits              | —          | 8    | —          | 9    | —           | 10   | —           | 12   | ns   |
| tACSS                | Chip Select Access Time Status Bits          | —          | 6    | —          | 7    | —           | 8    | —           | 10   | ns   |
| tSOH                 | Status Bit Hold from Address Change          | 2          | —    | 2          | —    | 2           | —    | 2           | —    | ns   |

**NOTE:**

1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

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## AC ELECTRICAL CHARACTERISTICS <sup>(1)</sup>

(V<sub>CC</sub> = 5.0V ± 5%, V<sub>CCQ</sub> = 5.0V ± 5% OR 3.3V ± 0.3V, T<sub>A</sub> = 0 to 70°C)

| Symbol                             | Parameter                         | IDT71216S8 |      | IDT71216S9 |      | IDT71216S10 |      | IDT71216S12 |      | Unit |
|------------------------------------|-----------------------------------|------------|------|------------|------|-------------|------|-------------|------|------|
|                                    |                                   | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.        | Max. |      |
| <b>Reset and Power Down Cycles</b> |                                   |            |      |            |      |             |      |             |      |      |
| tSR                                | RESET Set-up Time                 | 4          | —    | 4          | —    | 4           | —    | 4           | —    | ns   |
| tHR                                | RESET Hold Time                   | 1          | —    | 1          | —    | 1           | —    | 1           | —    | ns   |
| tSRST                              | Status Bit Reset Time             | —          | 50   | —          | 60   | —           | 60   | —           | 70   | ns   |
| tSHRS                              | Status Bit Hold from RESET LOW    | 2          | —    | 2          | —    | 2           | —    | 2           | —    | ns   |
| tRSMI                              | RESET LOW to MATCH and TA Invalid | —          | 9    | —          | 10   | —           | 10   | —           | 12   | ns   |
| tRSMV                              | RESET HIGH to MATCH and TA Valid  | —          | 110  | —          | 120  | —           | 120  | —           | 130  | ns   |
| tRSHZ <sup>(2)</sup>               | RESET LOW to TAG High-Z           | —          | 9    | —          | 10   | —           | 10   | —           | 12   | ns   |
| tRSLZ <sup>(2)</sup>               | RESET HIGH to TAG Low-Z           | —          | 90   | —          | 100  | —           | 100  | —           | 110  | ns   |
| tPDSR                              | PWRDN Set-up to RESET LOW         | 30         | —    | 30         | —    | 30          | —    | 30          | —    | ns   |
| tRHPL                              | RESET HIGH to PWRDN LOW           | 1          | —    | 1          | —    | 1           | —    | 1           | —    | CLK  |
| tRHWL                              | RESET HIGH to WET and WES LOW     | 90         | —    | 95         | —    | 95          | —    | 105         | —    | ns   |
| tPD <sup>(2)</sup>                 | PWRDN LOW to Low Power Mode       | —          | 50   | —          | 50   | —           | 50   | —           | 50   | ns   |
| tPU <sup>(2)</sup>                 | PWRDN HIGH to Active Power Mode   | 0          | —    | 0          | —    | 0           | —    | 0           | —    | ns   |
| tPDHZ <sup>(2)</sup>               | PWRDN LOW to Outputs in High-Z    | —          | 9    | —          | 10   | —           | 10   | —           | 12   | ns   |
| tPDLZ <sup>(2)</sup>               | PWRDN HIGH to Outputs in Low-Z    | 0          | —    | 0          | —    | 0           | —    | 0           | —    | ns   |
| tPUV                               | PWRDN HIGH to Outputs Valid       | —          | 50   | —          | 50   | —           | 50   | —           | 50   | ns   |
| tWHPL <sup>(2)</sup>               | WET and WES HIGH to PWRDN LOW     | 5          | —    | 5          | —    | 5           | —    | 5           | —    | ns   |
| tPUWL                              | PWRDN HIGH to WET and WES Active  | 50         | —    | 50         | —    | 50          | —    | 50          | —    | ns   |

**NOTES:**

1. Power-down mode is intended to be used during extended time periods of device inactivity.  
 2. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

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## AC ELECTRICAL CHARACTERISTICS (1)

(V<sub>CC</sub> = 5.0V ± 5%, V<sub>CCQ</sub> = 5.0V ± 5% OR 3.3V ± 0.3V, T<sub>A</sub> = 0 to 70°C)

| Symbol                                  | Parameter   | IDT71216S8 |      | IDT71216S9 |      | IDT71216S10 |      | IDT71216S12 |      | Unit |
|---|---|------------|------|------------|------|-------------|------|-------------|------|------|
|   |   | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.        | Max. |      |
| <b>Write Cycle and Clock Parameters</b> |   |            |      |            |      |             |      |             |      |      |
| t <sub>CYC</sub>                        | Clock Cycle Time  | 15         | —    | 15         | —    | 15          | —    | 16.6        | —    | ns   |
| t <sub>CH</sub> <sup>(2,3)</sup>        | Clock Pulse HIGH  | 4.5        | —    | 4.5        | —    | 4.5         | —    | 5           | —    | ns   |
| t <sub>CL</sub> <sup>(2,3)</sup>        | Clock Pulse LOW   | 4.5        | —    | 4.5        | —    | 4.5         | —    | 5           | —    | ns   |
| t <sub>S</sub>                          | $\overline{WET}$ , $\overline{WES}$ , Chip Select, and Input Data Set-up Time | 3          | —    | 3          | —    | 3           | —    | 3           | —    | ns   |
| t <sub>H</sub>                          | $\overline{WET}$ , $\overline{WES}$ , Chip Select, and Input Data Hold Time   | 1          | —    | 1          | —    | 1           | —    | 1           | —    | ns   |
| t <sub>SA</sub>                         | Address Set-up Time   | 3          | —    | 3          | —    | 3           | —    | 3           | —    | ns   |
| t <sub>HA</sub>                         | Address Hold Time   | 1          | —    | 1          | —    | 1           | —    | 1           | —    | ns   |
| t <sub>WMI</sub>                        | CLK HIGH Write to MATCH and $\overline{TA}$ Invalid                           | —          | 6    | —          | 7    | —           | 7    | —           | 8    | ns   |
| t <sub>CKLZ</sub> <sup>(3)</sup>        | CLK HIGH Read to Outputs in Low-Z   | 1.5        | —    | 1.5        | —    | 1.5         | —    | 1.5         | —    | ns   |
| t <sub>CTV</sub> <sup>(4)</sup>         | CLK HIGH Read to Tag Bits Valid   | —          | 9    | —          | 10   | —           | 10   | —           | 12   | ns   |
| t <sub>CSV</sub> <sup>(4)</sup>         | CLK HIGH Write to Status Outputs Valid  | —          | 8    | —          | 9    | —           | 9    | —           | 10   | ns   |
| t <sub>CSH</sub> <sup>(3)</sup>         | Status Output Hold from CLK HIGH Write  | 0          | —    | 0          | —    | 0           | —    | 0           | —    | ns   |
| t <sub>WHPL</sub>                       | $\overline{WET}$ and $\overline{WES}$ HIGH to $\overline{PWRDN}$ LOW          | 5          | —    | 5          | —    | 5           | —    | 5           | —    | ns   |
| t <sub>PUWL</sub>                       | $\overline{PWRDN}$ HIGH to $\overline{WET}$ and $\overline{WES}$ Active       | 50         | —    | 50         | —    | 50          | —    | 50          | —    | ns   |

**NOTES:**

1. All Write cycles are synchronous and referenced from rising CLK.
2. This parameter is measured as a HIGH time above 2.0V and a LOW time below 0.8V.
3. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
4. Addresses are stable prior to CLK transition HIGH.

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## AC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ± 5%, V<sub>CCQ</sub> = 5.0V ± 5% OR 3.3V ± 0.3V, T<sub>A</sub> = 0 to 70°C)

| Symbol  | Parameter   | IDT71216S8 |      | IDT71216S9 |      | IDT71216S10 |      | IDT71216S12 |      | Unit |
|---|---|------------|------|------------|------|-------------|------|-------------|------|------|
|   |   | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.        | Max. |      |
| <b>MATCH and <math>\overline{\text{TA}}</math> Cycles</b> |   |            |      |            |      |             |      |             |      |      |
| tADM  | Address to MATCH Valid  | —          | 8    | —          | 9    | —           | 10   | —           | 12   | ns   |
| tDAM  | Data Input to MATCH Valid   | —          | 8    | —          | 9    | —           | 10   | —           | 12   | ns   |
| tCSM  | Chip Select to MATCH Valid  | —          | 8    | —          | 9    | —           | 10   | —           | 12   | ns   |
| tCMLZ <sup>(1)</sup>                                      | Chip Select to MATCH in Low-Z   | 1          | —    | 1          | —    | 1           | —    | 1           | —    | ns   |
| tCMHZ <sup>(1)</sup>                                      | Chip Select to MATCH in High-Z  | 1          | 5    | 1          | 6    | 1           | 6    | 1           | 7    | ns   |
| tMHA  | MATCH Valid Hold from Address   | 2          | —    | 2          | —    | 2           | —    | 2           | —    | ns   |
| tMHD  | MATCH Valid Hold from Data  | 2          | —    | 2          | —    | 2           | —    | 2           | —    | ns   |
| tBHA  | $\overline{\text{TA}}$ Valid Hold from Address                          | 2          | —    | 2          | —    | 2           | —    | 2           | —    | ns   |
| tBHD  | $\overline{\text{TA}}$ Valid Hold from Data                             | 2          | —    | 2          | —    | 2           | —    | 2           | —    | ns   |
| tADB  | Address to $\overline{\text{TA}}$ Valid                                 | —          | 9    | —          | 10   | —           | 11   | —           | 13   | ns   |
| tDAB  | Data Input to $\overline{\text{TA}}$ Valid                              | —          | 9    | —          | 10   | —           | 11   | —           | 13   | ns   |
| tCSB  | Chip Select LOW to $\overline{\text{TA}}$ Valid                         | —          | 9    | —          | 10   | —           | 11   | —           | 13   | ns   |
| toEBV   | $\overline{\text{TAOE}}$ LOW to $\overline{\text{TA}}$ Valid            | —          | 6    | —          | 6    | —           | 7    | —           | 8    | ns   |
| toBLZ <sup>(1)</sup>                                      | $\overline{\text{TAOE}}$ LOW to $\overline{\text{TA}}$ in Low-Z         | 0          | —    | 0          | —    | 0           | —    | 0           | —    | ns   |
| toBHZ <sup>(1)</sup>                                      | $\overline{\text{TAOE}}$ HIGH to $\overline{\text{TA}}$ in High-Z       | 1          | 5    | 1          | 6    | 1           | 6    | 1           | 7    | ns   |
| tBYFH   | TAH HIGH to Force $\overline{\text{TA}}$ HIGH                           | —          | 5    | —          | 5    | —           | 5    | —           | 6    | ns   |
| tBYHV   | TAH LOW to $\overline{\text{TA}}$ Valid                                 | —          | 5    | —          | 5    | —           | 5    | —           | 6    | ns   |
| tSB   | $\overline{\text{TAIN}}$ Set-up Time                                    | 4          | —    | 4          | —    | 4           | —    | 4           | —    | ns   |
| tHB   | $\overline{\text{TAIN}}$ Hold Time                                      | 1.5        | —    | 1.5        | —    | 1.5         | —    | 1.5         | —    | ns   |
| tBIBL   | CLK HIGH $\overline{\text{TAIN}}$ LOW to $\overline{\text{TA}}$ LOW     | —          | 6    | —          | 6    | —           | 7    | —           | 8    | ns   |
| tBIBV   | CLK HIGH $\overline{\text{TAIN}}$ HIGH to $\overline{\text{TA}}$ Valid  | —          | 6    | —          | 6    | —           | 7    | —           | 8    | ns   |
| toEMI   | $\overline{\text{OET}}$ LOW to MATCH and $\overline{\text{TA}}$ Invalid | —          | 6    | —          | 7    | —           | 7    | —           | 8    | ns   |
| toEMV   | $\overline{\text{OET}}$ HIGH to MATCH and $\overline{\text{TA}}$ Valid  | —          | 7    | —          | 8    | —           | 8    | —           | 10   | ns   |
| tWRBH <sup>(2)</sup>                                      | W/ $\overline{\text{R}}$ HIGH to $\overline{\text{TA}}$ HIGH            | —          | 6    | —          | 7    | —           | 7    | —           | 8    | ns   |
| tWRBV <sup>(2)</sup>                                      | W/ $\overline{\text{R}}$ LOW to $\overline{\text{TA}}$ Valid            | —          | 6    | —          | 7    | —           | 7    | —           | 8    | ns   |
| tWMI  | CLK HIGH Write to MATCH and $\overline{\text{TA}}$ Invalid              | —          | 7    | —          | 7    | —           | 7    | —           | 8    | ns   |
| tWMV <sup>(3)</sup>                                       | CLK HIGH Read to MATCH and $\overline{\text{TA}}$ Valid                 | —          | 8    | —          | 9    | —           | 10   | —           | 12   | ns   |

**NOTES:**

1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
2. These parameters only apply when SFUNC is LOW and the internal WT bit is HIGH.
3. tADM, tDAM, tCSM and tADB, tDAB, tCSB must also be satisfied.

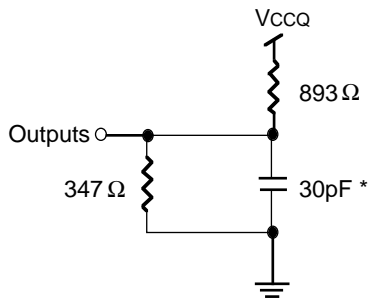
3067 tbl 15

## AC TEST CONDITIONS

|                                |                        |
|--------------------------------|------------------------|
| Input Pulse Levels             | GND to 3.0V            |
| Input Rise/Fall Times          | 3ns                    |
| Input Timing Reference Levels  | 1.5V                   |
| Output Timing Reference Levels | 1.5V                   |
| AC Test Load                   | See Figs. 1, 2, 3, & 4 |

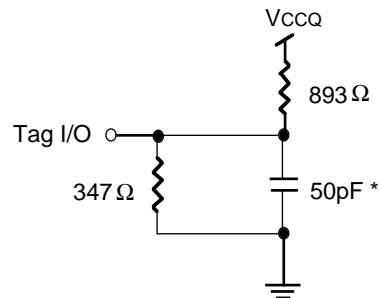
3067 tbl 16

## AC TEST LOADS



3067 drw 03

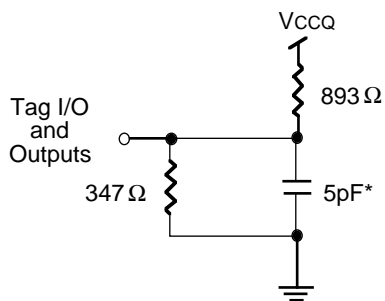
Figure 1. AC Test Load



3067 drw 04

Figure 2. Tag I/O AC Test Load

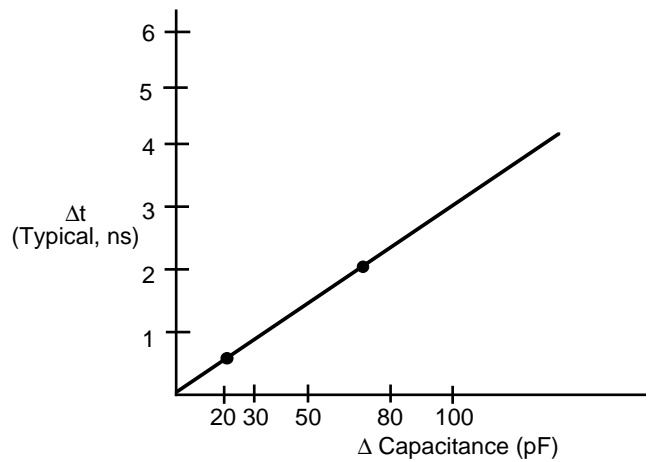
\* Including scope and jig capacitance



3067 drw 05

Figure 3. AC Test Load  
(for thz and tLZ parameters)

\* Including scope and jig capacitance



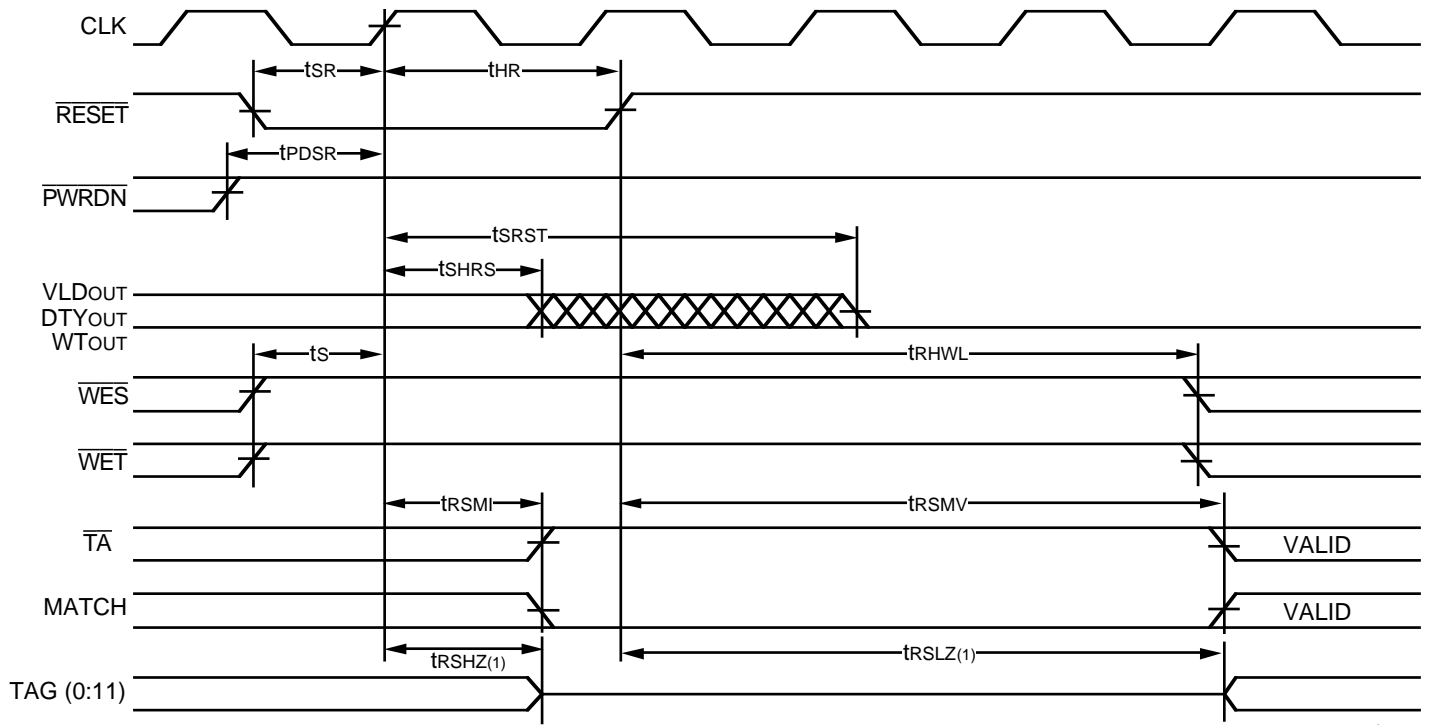
3067 drw 06

Figure 4. Lumped Capacitance Load, Typical Derating





### TIMING WAVEFORMS OF RESET FUNCTION

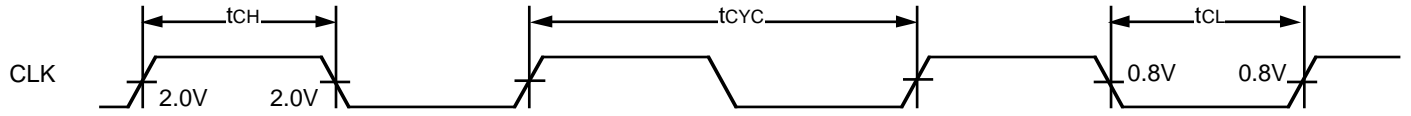


3067 drw 09

**NOTE:**

1. Transition is measured  $\pm 200\text{mV}$  from steady state.

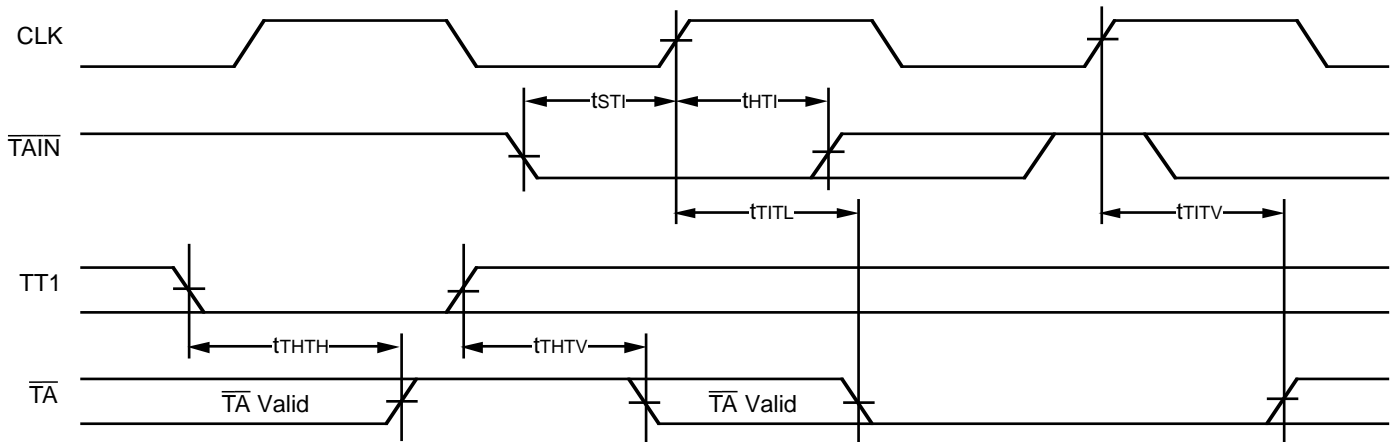
### CLOCK TIMING WAVEFORM



3067 drw 10

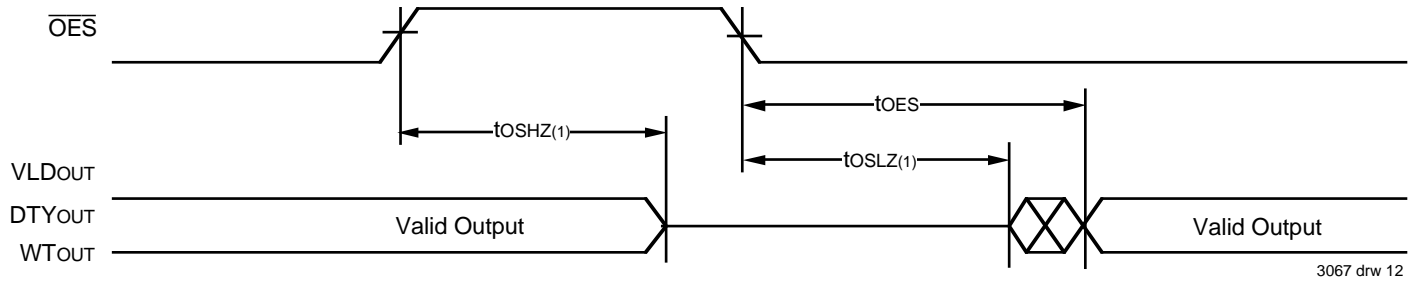
### TIMING WAVEFORMS OF TA AND TT1 SIGNAL

Applies when SFUNC is LOW, and the internal WT bit is HIGH



3067 drw 11

### TIMING WAVEFORMS OF $\overline{OES}$ FUNCTION

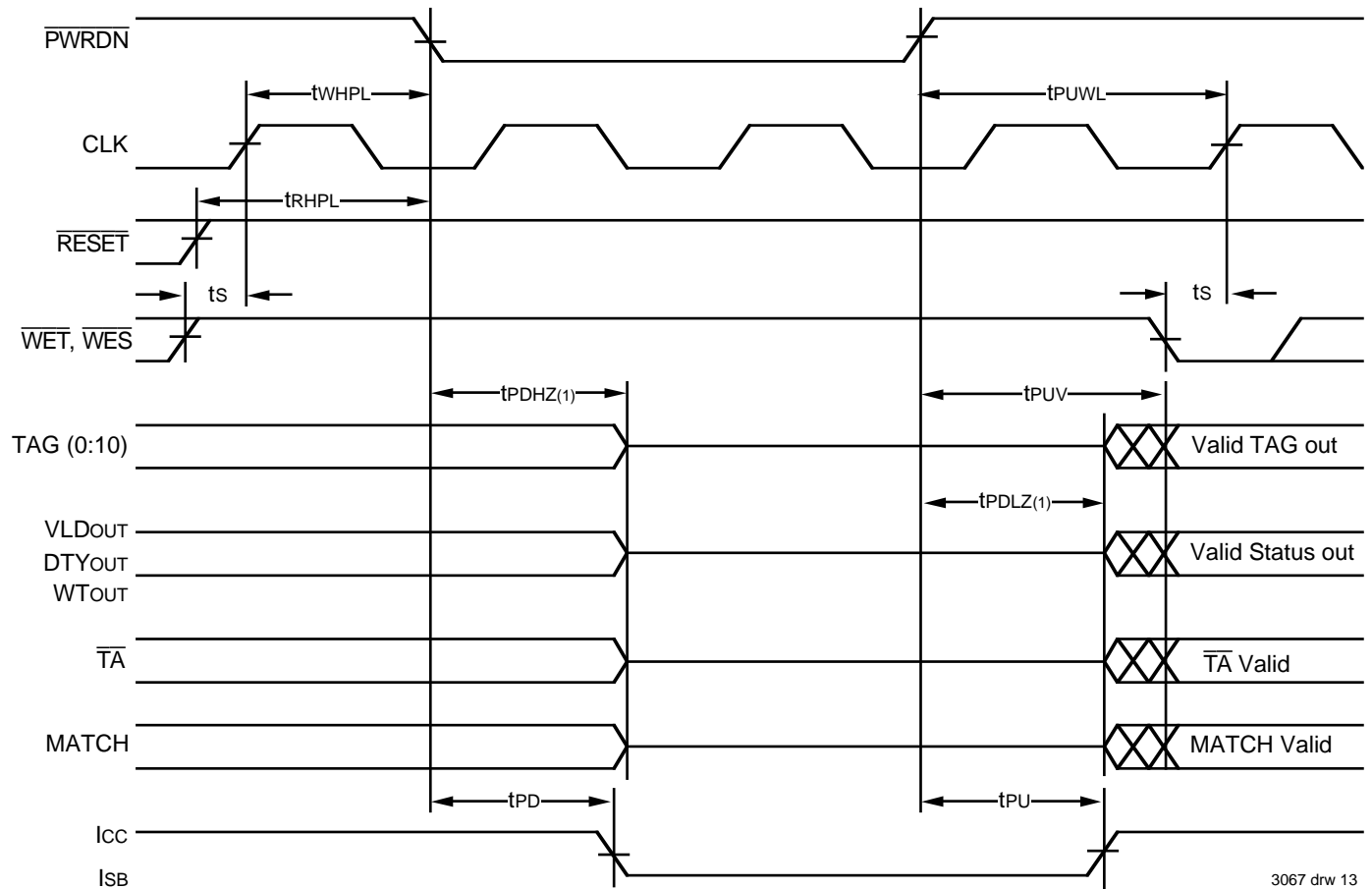


3067 drw 12

**NOTE:**

1. Transition is measured  $\pm 200\text{mV}$  from steady state.

### TIMING WAVEFORMS OF POWER DOWN FUNCTION



3067 drw 13

**NOTE:**

1. Transition is measured  $\pm 200\text{mV}$  from steady state.

### ORDERING INFORMATION

|     |              |          |           |           |                                     |
|-----|--------------|----------|-----------|-----------|-------------------------------------|
| IDT | <u>71216</u> | <u>S</u> | <u>XX</u> | <u>PF</u> |                                     |
|     | Device Type  | Power    | Speed     | Package   |                                     |
|     |              |          |           | PF        | Plastic Thin Quad Flatpack (PN80-1) |
|     |              |          |           | 8         | } Speed in nanoseconds              |
|     |              |          |           | 9         |                                     |
|     |              |          |           | 10        |                                     |
|     |              |          |           | 12        |                                     |

3067 drw 14