

## Features

- Fast Read Access Time - 90 ns
- Dual Voltage Range Operation
  - Low Voltage Power Supply Range, 3.0V to 3.6V
  - or Standard 5V ± 10% Supply Range
- Compatible with JEDEC Standard AT27C512
- Low Power CMOS Operation
  - 20 μA max. (less than 1 μA typical) Standby for V<sub>CC</sub> = 3.6V
  - 29 mW max. Active at 5 MHz for V<sub>CC</sub> = 3.6V
- JEDEC Standard Packages
  - 32-Lead PLCC
  - 28-Lead 330-mil SOIC
  - 28-Lead TSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 μs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTTL
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

## Description

The AT27LV512A is a high performance, low power, low voltage 524,288 bit one-time programmable read only memory (OTP EPROM) organized as 64K by 8 bits. It requires only one supply in the range of 3.0V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

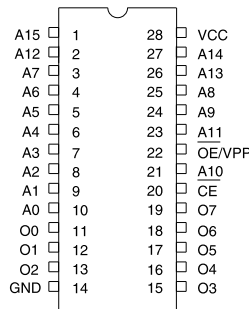
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3.3V supply. At V<sub>CC</sub> = 3.0V, any byte can be accessed in less than 90 ns. With a typical power dissipation of only 18 mW at 5 MHz and V<sub>CC</sub> = 3.3V, the AT27LV512A consumes less than one fifth the power of a standard 5V EPROM.

(continued)

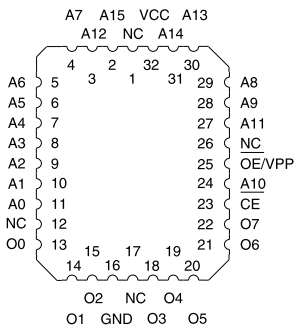
## Pin Configurations

Pin Name	Function
A0 - A15	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable
NC	No Connect

SOIC Top View

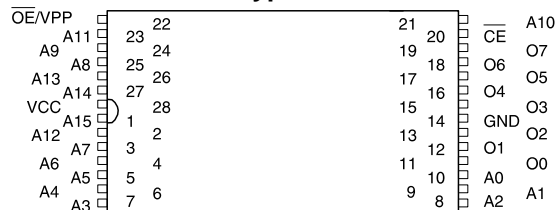


PLCC Top View



TSOP Top View

Type 1



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

# 512K (64K x 8) Low Voltage OTP CMOS EPROM

## Description (Continued)

Standby mode supply current is typically less than 1  $\mu\text{A}$  at 3.3V.

The AT27LV512A is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC, SOIC, and TSOP packages. All devices feature two-line control ( $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ ) to give designers the flexibility to prevent bus contention.

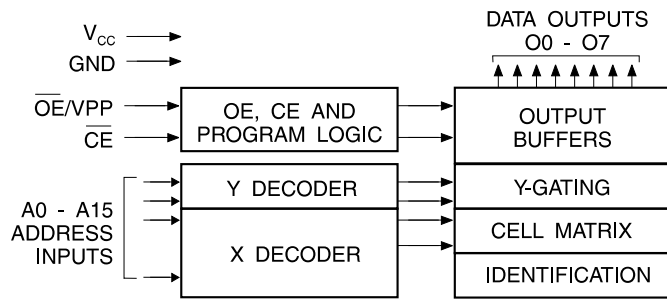
The AT27LV512A operating with  $V_{\text{CC}}$  at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at  $V_{\text{CC}} = 5.0\text{V}$ . The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27LV512A has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100  $\mu\text{s}/\text{byte}$ . The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV512A programs exactly the same way as a standard 5V AT27C512R and uses the same programming equipment.

## System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu\text{F}$  high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{\text{CC}}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu\text{F}$  bulk electrolytic capacitor should be utilized, again connected between the  $V_{\text{CC}}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature Under Bias .....	-40°C to +85°C
Storage Temperature.....	-65°C to +125°C
Voltage on Any Pin with Respect to Ground.....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
V <sub>PP</sub> Supply Voltage with Respect to Ground.....	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V<sub>CC</sub> + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 volts for pulses of less than 20 ns.

## Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE/V_{PP}}$	A <sub>i</sub>	V <sub>CC</sub>	Outputs
Read <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	A <sub>i</sub>	V <sub>CC</sub> <sup>(2)</sup>	DOUT
Output Disable <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	X <sup>(1)</sup>	V <sub>CC</sub> <sup>(2)</sup>	High Z
Standby <sup>(2)</sup>	V <sub>IH</sub>	X	X	V <sub>CC</sub> <sup>(2)</sup>	High Z
Rapid Program <sup>(3)</sup>	V <sub>IL</sub>	V <sub>PP</sub>	A <sub>i</sub>	V <sub>CC</sub> <sup>(3)</sup>	DIN
PGM Inhibit <sup>(3)</sup>	V <sub>IH</sub>	V <sub>PP</sub>	X	V <sub>CC</sub> <sup>(3)</sup>	High Z
Product Identification <sup>(3, 5)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	A <sub>9</sub> = V <sub>H</sub> <sup>(4)</sup> A <sub>0</sub> = V <sub>IH</sub> or V <sub>IL</sub> A <sub>1</sub> - A <sub>15</sub> = V <sub>IL</sub>	V <sub>CC</sub> <sup>(3)</sup>	Identification Code

Notes: 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.  
 2. Read, output disable, and standby modes require, 3.0V ≤ V<sub>CC</sub> ≤ 3.6V, or 4.5V ≤ V<sub>CC</sub> ≤ 5.5V.  
 3. Refer to Programming Characteristics. Programming modes require V<sub>CC</sub> = 6.5V.

4. V<sub>H</sub> = 12.0 ± 0.5V.  
 5. Two identifier bytes may be selected. All A<sub>i</sub> inputs are held low (V<sub>IL</sub>), except A<sub>9</sub> which is set to V<sub>H</sub> and A<sub>0</sub> which is toggled low (V<sub>IL</sub>) to select the Manufacturer's Identification byte and high (V<sub>IH</sub>) to select the Device Code byte.

## DC and AC Operating Conditions for Read Operation

		AT27LV512A		
		-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Power Supply		3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

## DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
<b>V<sub>CC</sub> = 3.0V to 3.6V</b>					
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>		±1	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>		±5	μA
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	V <sub>PP</sub> = V <sub>CC</sub>		10	μA
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		20	μA
		I <sub>SB2</sub> (TTL), $\overline{CE} = 2.0$ to V <sub>CC</sub> + 0.5V		100	μA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz, I <sub>OUT</sub> = 0 mA, CE = V <sub>IL</sub>		8	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.0 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2.0 mA	2.4		V
<b>V<sub>CC</sub> = 4.5V to 5.5V</b>					
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>		±1	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>		±5	μA
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	V <sub>PP</sub> = V <sub>CC</sub>		10	μA
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I <sub>SB2</sub> (TTL), $\overline{CE} = 2.0$ to V <sub>CC</sub> + 0.5V		1	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz, I <sub>OUT</sub> = 0 mA, CE = V <sub>IL</sub>		20	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

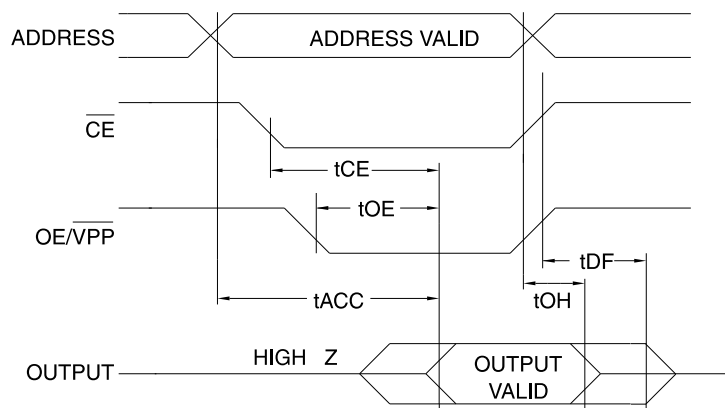
Note: 1. V<sub>CC</sub> must be applied simultaneously with or before  $\overline{OE}/V_{PP}$ , and removed simultaneously with or after  $\overline{OE}/V_{PP}$ .

## AC Characteristics for Read Operation ( $V_{CC} = 3.0V$ to $3.6V$ and $4.5V$ to $5.5V$ )

Symbol	Parameter	Condition	-90		-12		-15		Units
			Min	Max	Min	Max	Min	Max	
$t_{ACC}^{(3)}$	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		90		120		150	ns
$t_{CE}^{(2)}$	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$		90		120		150	ns
$t_{OE}^{(2,3)}$	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE} = V_{IL}$		50		50		60	ns
$t_{DF}^{(4,5)}$	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, whichever occurred first			40		40		50	ns
$t_{OH}$	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ , whichever occurred first		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

## AC Waveforms for Read Operation <sup>(1)</sup>

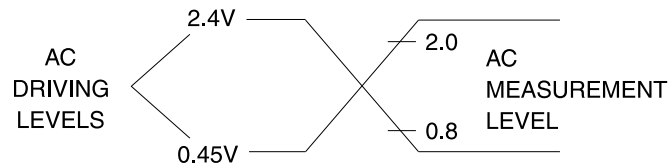


Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.

2.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
3.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .

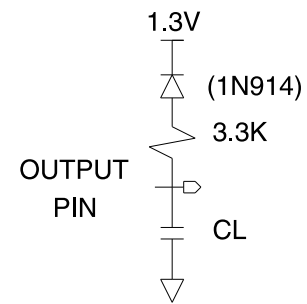
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

## Input Test Waveform and Measurement Level



$t_R, t_F < 20$  ns (10% to 90%)

## Output Test Load



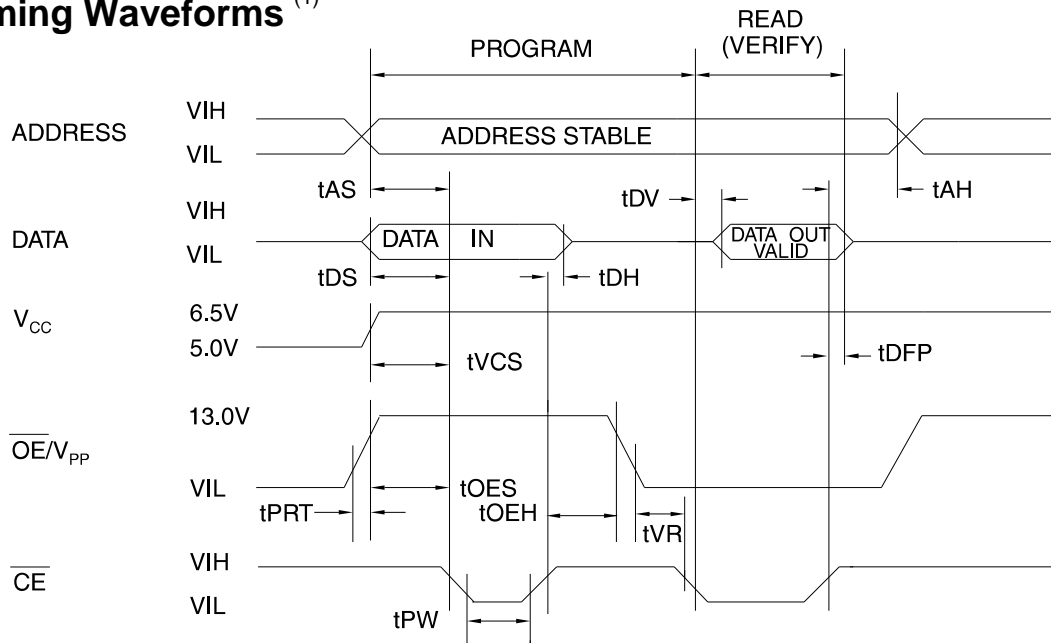
Note: CL = 100 pF including jig capacitance.

## Pin Capacitance ( $f = 1$ MHz, $T = 25^\circ\text{C}$ )<sup>(1)</sup>

	Typ	Max	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

### Programming Waveforms <sup>(1)</sup>



- Notes: 1. The Input Timing Reference is 0.8V for V<sub>IL</sub> and 2.0V for V<sub>IH</sub>.  
 2. t<sub>OE</sub> and t<sub>DFP</sub> are characteristics of the device but must be accommodated by the programmer.

### DC Programming Characteristics

T<sub>A</sub> = 25 ± 5°C, V<sub>CC</sub> = 6.5 ± 0.25V, OE/V<sub>PP</sub> = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = V <sub>IL</sub> , V <sub>IH</sub>		10	μA
V <sub>IL</sub>	Input Low Level		-0.6	0.8	V
V <sub>IH</sub>	Input High Level		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Program and Verify)			25	mA
I <sub>PP2</sub>	OE/V <sub>PP</sub> Current	CE = V <sub>IL</sub>		25	mA
V <sub>ID</sub>	A9 Product Identification Voltage		11.5	12.5	V

## AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $\overline{OE}/V_{PP} = 13.0 \pm 0.25\text{V}$

Sym- bol	Parameter	Test Conditions* (1)	Limits		Units
			Min	Max	
t <sub>AS</sub>	Address Setup Time		2		μs
t <sub>OES</sub>	$\overline{OE}/V_{PP}$ Setup Time		2		μs
t <sub>OEH</sub>	$\overline{OE}/V_{PP}$ Hold Time		2		μs
t <sub>DS</sub>	Data Setup Time		2		μs
t <sub>AH</sub>	Address Hold Time		0		μs
t <sub>DH</sub>	Data Hold Time		2		μs
t <sub>DFP</sub>	$\overline{CE}$ High to Output Float Delay (2)		0	130	ns
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time		2		μs
t <sub>PW</sub>	$\overline{CE}$ Program Pulse Width (3)		95	105	μs
t <sub>DV</sub>	Data Valid from $\overline{CE}$ (2)			1	μs
t <sub>VR</sub>	$\overline{OE}/V_{PP}$ Recovery Time		2		μs
t <sub>PRT</sub>	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

### \*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns  
 Input Pulse Levels.....0.45V to 2.4V  
 Input Timing Reference Level.....0.8V to 2.0V  
 Output Timing Reference Level.....0.8V to 2.0V

- Notes: 1.  $V_{CC}$  must be applied simultaneously or before  $\overline{OE}/V_{PP}$  and removed simultaneously or after  $\overline{OE}/V_{PP}$ .  
 2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.  
 3. Program Pulse width tolerance is 100 μsec ± 5%.

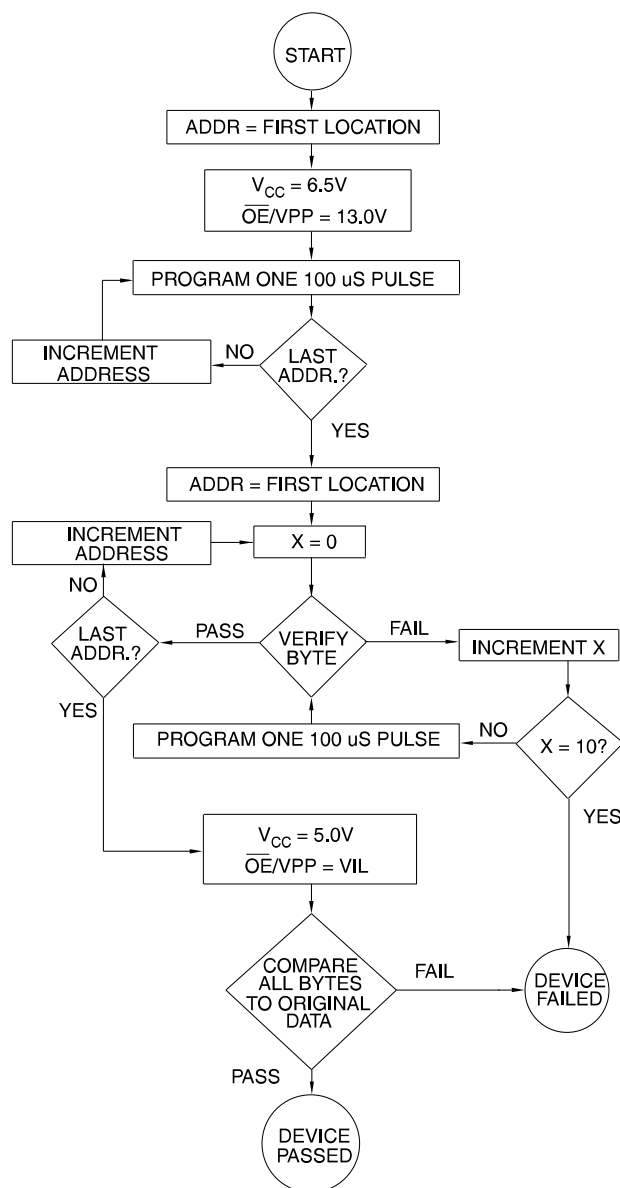
## Atmel's 27LV512A Integrated Product Identification Code (1)

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	0D

Note: 1. The AT27LV512A has the same Product Identification Code as the AT27C512R. Both are programming compatible.

## Rapid Programming Algorithm

A 100 μs  $\overline{CE}$  pulse width is used to program. The address is set to the first location.  $V_{CC}$  is raised to 6.5V and  $\overline{OE}/V_{PP}$  is raised to 13.0V. Each address is first programmed with one 100 μs  $\overline{CE}$  pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $\overline{OE}/V_{PP}$  is then lowered to  $V_{IL}$  and  $V_{CC}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.





## Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	8	0.02	AT27LV512A-90JC AT27LV512A-90RC AT27LV512A-90TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV512A-90JI AT27LV512A-90RI AT27LV512A-90TI	32J 28R 28T	Industrial (-40°C to 85°C)
120	8	0.02	AT27LV512A-12JC AT27LV512A-12RC AT27LV512A-12TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV512A-12JI AT27LV512A-12RI AT27LV512A-12TI	32J 28R 28T	Industrial (-40°C to 85°C)
150	8	0.02	AT27LV512A-15JC AT27LV512A-15RC AT27LV512A-15TC	32J 28R 28T	Commercial (0°C to 70°C)
	8	0.02	AT27LV512A-15JI AT27LV512A-15RI AT27LV512A-15TI	32J 28R 28T	Industrial (-40°C to 85°C)

Package Type	
<b>32J</b>	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
<b>28R</b>	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
<b>28T</b>	28 Lead, Thin Small Outline Package (TSOP)