DSP Microcomputer

ADSP-21065L

SUMMARY

High Performance Signal Computer for Communications, Audio, Automotive, Instrumentation and Industrial Applications

Super Harvard Architecture Computer (SHARC®)
Four Independent Buses for Dual Data, Instruction, and I/O Fetch on a Single Cycle

32-Bit Fixed-Point Arithmetic; 32-Bit and 40-Bit Floating-Point Arithmetic

544 Kbits On-Chip SRAM Memory and Integrated I/O Peripheral

I^2S Support, for Eight Simultaneous Receive and Transmit Channels

KEY FEATURES

66 MIPS, 198 MFLOPS Peak, 132 MFLOPS Sustained Performance

User-Configurable 544 Kbits On-Chip SRAM Memory

Two External Port, DMA Channels and Eight Serial Port, DMA Channels

SDRAM Controller for Glueless Interface to Low Cost External Memory (@ 66 MHz)

64M Words External Address Range

12 Programmable I/O Pins and Two Timers with Event Capture Options

Code-Compatible with ADSP-2106x Family

208-Lead MQFP or 196-Ball Mini-BGA Package

3.3 Volt Operation

Flexible Data Formats and 40-Bit Extended Precision

32-Bit Single-Precision and 40-Bit Extended-Precision IEEE Floating-Point Data Formats

32-Bit Fixed-Point Data Format, Integer and Fractional, with Dual 80-Bit Accumulators

Parallel Computations

Single-Cycle Multiply and ALU Operations in Parallel with Dual Memory Read/Writes and Instruction Fetch

Multiply with Add and Subtract for Accelerated FFT Butterfly Computation

1024-Point Complex FFT Benchmark: 0.274 ms (18,221 Cycles)

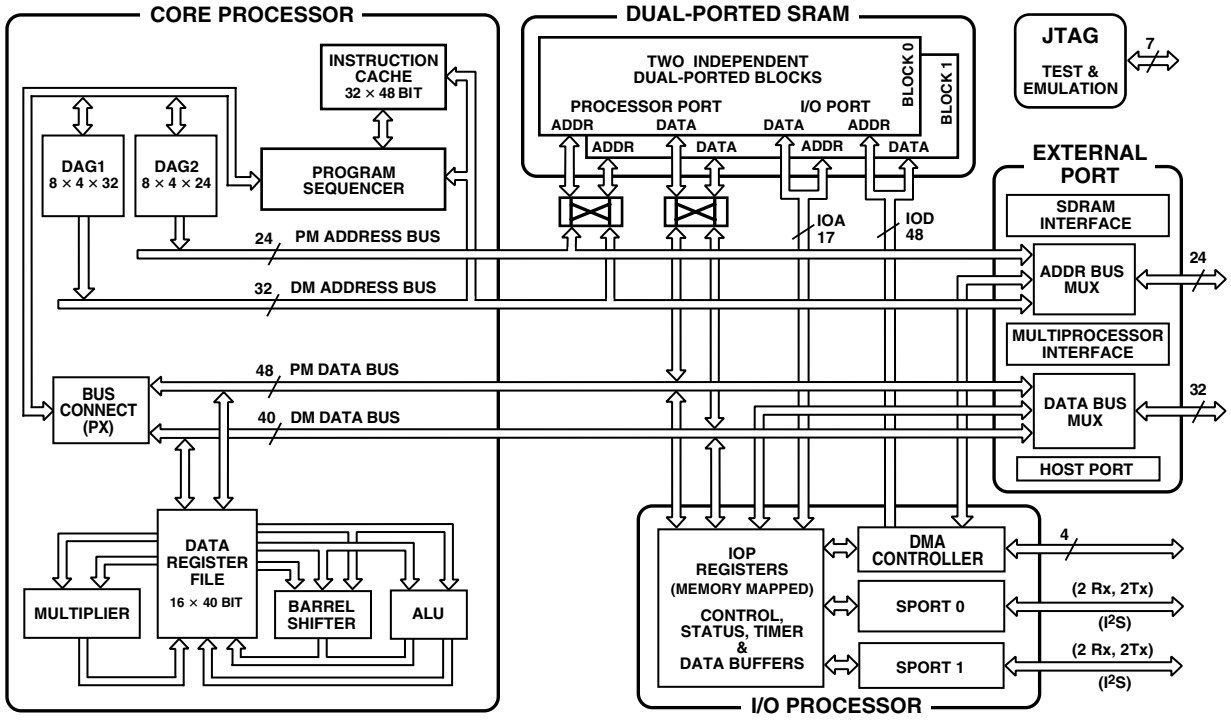


Figure 1. Functional Block Diagram

SHARC is a registered trademark of Analog Devices, Inc.

REV. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
© Analog Devices, Inc., 2000

544 Kbits Configurable On-Chip SRAM

Dual-Ported for Independent Access by Core Processor and DMA

Configurable in Combinations of 16-, 32-, 48-Bit Data and Program Words in Block 0 and Block 1

DMA Controller

Ten DMA Channels—Two Dedicated to the External Port and Eight Dedicated to the Serial Ports

Background DMA Transfers at up to 66 MHz, in Parallel with Full Speed Processor Execution

Performs Transfers Between:

- **Internal RAM and Host**
- **Internal RAM and Serial Ports**
- **Internal RAM and Master or Slave SHARC**
- **Internal RAM and External Memory or I/O Devices**
- **External Memory and External Devices**

Host Processor Interface

Efficient Interface to 8-, 16-, and 32-Bit Microprocessors

Host Can Directly Read/Write ADSP-21065L IOP Registers

Multiprocessing

Distributed On-Chip Bus Arbitration for Glueless, Parallel Bus Connect Between Two ADSP-21065Ls Plus Host

132 Mbytes/s Transfer Rate Over Parallel Bus

Serial Ports

Independent Transmit and Receive Functions

Programmable 3-Bit to 32-Bit Serial Word Width

I^2S Support Allowing Eight Transmit and Eight Receive Channels

Glueless Interface to Industry Standard Codecs

TDM Multichannel Mode with μ-Law/A-Law Hardware Companding

Multichannel Signaling Protocol

GENERAL DESCRIPTION

The ADSP-21065L is a powerful member of the SHARC family of 32-bit processors optimized for cost sensitive applications. The SHARC—Super Harvard Architecture—offers the highest levels of performance and memory integration of any 32-bit DSP in the industry—they are also the only DSP in the industry that offer both fixed and floating-point capabilities, without compromising precision or performance.

Fabricated in a high speed, low power CMOS process, 0.35 µm technology, the ADSP-21065L offers the highest performance by a 32-bit DSP—66 MIPS (198 MFLOPS). With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table I lists the performance benchmarks for the ADSP-21065L.

The ADSP-21065L SHARC combines a floating-point DSP core with integrated, on-chip system features, including a 544 Kbit SRAM memory, host processor interface, DMA controller, SDRAM controller, and enhanced serial ports.

Figure 1 shows a block diagram of the ADSP-21065L, illustrating the following architectural features:

- Computation Units (ALU, Multiplier, and Shifter) with a Shared Data Register File
- Data Address Generators (DAG1, DAG2)
- Program Sequencer with Instruction Cache
- Timers with Event Capture Modes
- On-Chip, dual-ported SRAM
- External Port for Interfacing to Off-Chip Memory and Peripherals
- Host Port and SDRAM Interface
- DMA Controller
- Enhanced Serial Ports
- JTAG Test Access Port

Table I. Performance Benchmarks

Benchmark	Timing	Cycles
Cycle Time	15.00 ns	1
1024-Pt. Complex FFT (Radix 4, with Digit Reverse)	0.274 ns	18221
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	135 ns	9
[4 × 4] × [4 × 1]	240 ns	16
FIR Filter (per Tap)	15 ns	1
IIR Filter (per Biquad)	60 ns	4
Divide Y/X	90 ns	6
Inverse Square Root ($1/\sqrt{x}$)	135 ns	9
DMA Transfers	264 Mbytes/sec.	

ADSP-21000 FAMILY CORE ARCHITECTURE

The ADSP-21065L is code and function compatible with the ADSP-21060/ADSP-21061/ADSP-21062. The ADSP-21065L includes the following architectural features of the SHARC family core.

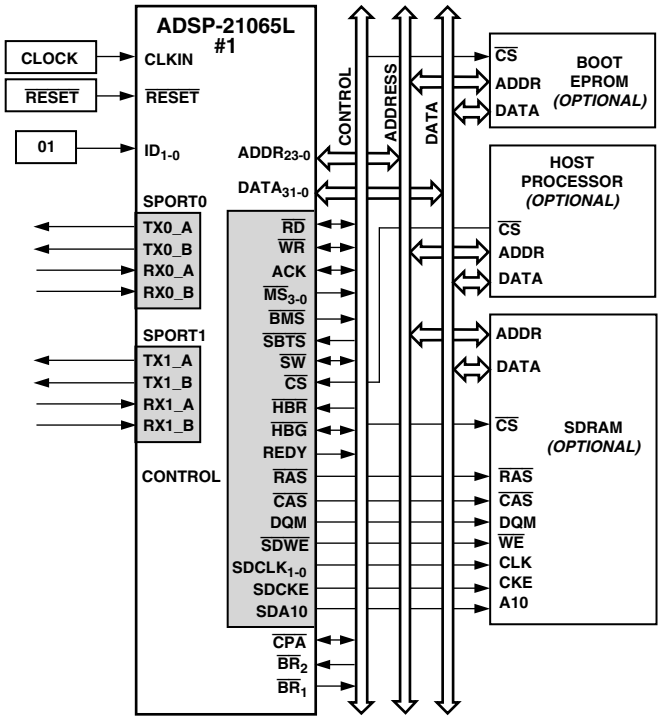


Figure 2. ADSP-21065L Single-Processor System

Independent, Parallel Computation Units

The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands

The ADSP-21065L features an enhanced Super Harvard Architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1). With its separate program and data memory buses, and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21065L includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions that fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-21065L's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data

structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The ADSP-21065L's two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set
The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21065L can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

ADSP-21065L FEATURES

The ADSP-21065L is designed to achieve the highest system throughput to enable maximum system performance. It can be clocked by either a crystal or a TTL-compatible clock signal. The ADSP-21065L uses an input clock with a frequency equal to half the instruction rate—a 33 MHz input clock yields a 15 ns processor cycle (which is equivalent to 66 MHz). Interfaces on the ADSP-21065L operate as shown below. Hereafter in this document, 1x = input clock frequency, and 2x = processor's instruction rate.

The following clock operation ratings are based on 1x = 33 MHz (instruction rate/core = 66 MHz):

SDRAM	66 MHz
External SRAM	33 MHz
Serial Ports	33 MHz
Multiprocessing	33 MHz
Host (Asynchronous)	33 MHz

Augmenting the ADSP-21000 family core, the ADSP-21065L adds the following architectural features:

Dual-Ported On-Chip Memory
The ADSP-21065L contains 544 Kbits of on-chip SRAM, organized into two banks: Bank 0 has 288 Kbits, and Bank 1 has 256 Kbits. Bank 0 is configured with 9 columns of 2K × 16 bits, and Bank 1 is configured with 8 columns of 2K × 16 bits. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21065L Memory Map).

On the ADSP-21065L, the memory can be configured as a maximum of 16K words of 32-bit data, 34K words for 16-bit data, 10K words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 544 Kbits. All the memory can be accessed as 16-bit, 32-bit or 48-bit.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM and PM busses in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-21065L's external port.

Off-Chip Memory and Peripherals Interface
The ADSP-21065L's external port provides the processor's interface to off-chip memory and peripherals. The 64M words, off-chip address space is included in the ADSP-21065L's unified address space. The separate on-chip buses—for program memory, data memory and I/O—are multiplexed at the external port to create an external system bus with a single 24-bit address bus, four memory selects, and a single 32-bit data bus. The on-chip Super Harvard Architecture provides three bus performance, while the off-chip unified address space gives flexibility to the designer.

SDRAM Interface
The SDRAM interface enables the ADSP-21065L to transfer data to and from synchronous DRAM (SDRAM) at 2x clock frequency. The synchronous approach coupled with 2x clock frequency supports data transfer at a high throughput—up to 220 Mbytes/sec.

The SDRAM interface provides a glueless interface with standard SDRAMs—16 Mb, 64 Mb, and 128 Mb—and includes options to support additional buffers between the ADSP-21065L and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21065L's four external memory banks.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21065L supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Host Processor Interface
The ADSP-21065L's host interface provides easy connection to standard microprocessor buses—8-, 16-, and 32-bit—requiring little additional hardware. Supporting asynchronous transfers at speeds up to 1x clock frequency, the host interface is accessed through the ADSP-21065L's external port. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21065L's external bus with the host bus request ($\overline{HBR}$), host bus grant ($\overline{HBG}$), and ready (REDY) signals. The host can directly read and write the IOP registers of the ADSP-21065L and can access the DMA channel setup and mailbox registers. Vector interrupt support enables efficient execution of host commands.

DMA Controller
The ADSP-21065L's on-chip DMA controller allows zero-overhead, nonintrusive data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-21065L's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21065L's internal memory and its serial ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit internal words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-21065L—eight via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21065L, memory or

I/O transfers). Programs can be downloaded to the ADSP-21065L using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation on completion of DMA transfers and DMA chaining for automatically linked DMA transfers.

Serial Ports

The ADSP-21065L features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at 1x clock frequency, providing each with a maximum data rate of 33 Mbit/s. Each serial port has a primary and a secondary set of transmit and receive channels. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports supports three operation modes: DSP serial port mode, I^2S mode (an interface commonly used by audio codecs), and TDM (Time Division Multiplex) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with selectable word lengths of 3 bits to 32 bits. They offer selectable synchronization and transmit modes and optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and keymask features to enhance interprocessor communication.

Programmable Timers and General Purpose I/O Ports

The ADSP-21065L has two independent timer blocks, each of which performs two functions—Pulsewidth Generation and Pulse Count and Capture.

In Pulsewidth Generation mode, the ADSP-21065L can generate a modulated waveform with an arbitrary pulsewidth within a maximum period of 71.5 secs.

In Pulse Counter mode, the ADSP-21065L can measure either the high or low pulsewidth and the period of an input waveform.

The ADSP-21065L also contains twelve programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting

The internal memory of the ADSP-21065L can be booted at system power-up from an 8-bit EPROM, a host processor, or external memory. Selection of the boot source is controlled by the $\overline{BMS}$ (Boot Memory Select) and BSEL (EPROM Boot) pins. Either 8-, 16-, or 32-bit host processors can be used for booting. For details, see the descriptions of the $\overline{BMS}$ and BSEL pins in the Pin Descriptions section of this data sheet.

Multiprocessing

The ADSP-21065L offers powerful features tailored to multiprocessing DSP systems. The unified address space allows direct interprocessor accesses of both ADSP-21065L's IOP registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing a maximum of two ADSP-21065Ls and a host processor. Master processor changeover incurs only one cycle of overhead. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 132 Mbytes/sec over the external port.

DEVELOPMENT TOOLS

The ADSP-21065L is supported with a complete set of software and hardware development tools, including the EZ-ICE® In-Circuit Emulator and development software.

The same EZ-ICE hardware that you use for the ADSP-21060/ADSP-21062 also fully emulates the ADSP-21065L.

Both the SHARC Development Tools family and the VisualDSP® integrated project management and debugging environment support the ADSP-21065L. The VisualDSP project management environment enables you to develop and debug an application from within a single integrated program.

The SHARC Development Tools include an easy to use Assembler that is based on an algebraic syntax; an Assembly library/librarian; a linker; a loader; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and Assembly programs with the Visual DSP debugger, you can:

- View Mixed C and Assembly Code
- Insert Break Points
- Set Watch Points
- Trace Bus Activity
- Profile Program Execution
- Fill and Dump Memory
- Create Custom Debugger Windows

The Visual IDE enables you to define and manage multiuser projects. Its dialog boxes and property pages enable you to configure and manage all of the SHARC Development Tools. This capability enables you to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-21065L processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards multiprocessor SHARC VME boards, and daughter and modules with multiple SHARCs and additional memory. These modules are based on the SHARCPAC™ module specification. Third Party software tools include an Ada compiler, DSP libraries, operating systems, and block diagram design tools.

Additional Information

For detailed information on the ADSP-21065L instruction set and architecture, see the *ADSP-21065L SHARC User's Manual*, Third Edition, and the *ADSP-21065L SHARC Technical Reference.*

EZ-ICE and VisualDSP are registered trademarks of Analog Devices, Inc.
SHARCPAC is a trademark of Analog Devices Inc.

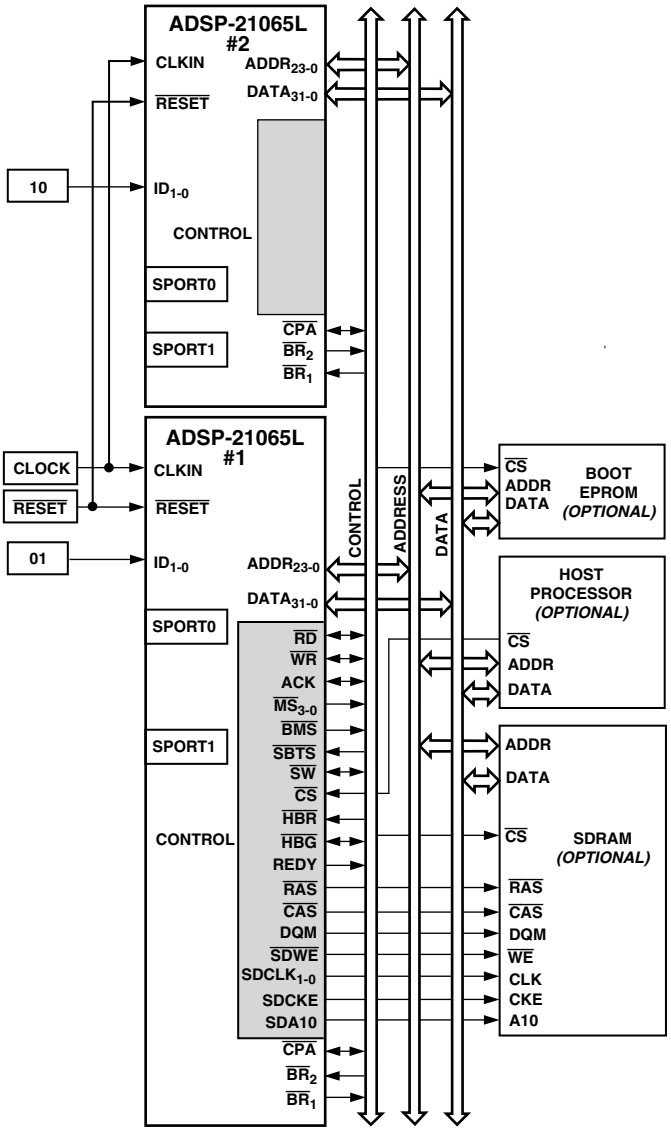


Figure 3. Multiprocessing System

PIN DESCRIPTIONS

ADSP-21065L pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for $\text{ADDR}_{23\text{-}0}$, $\text{DATA}_{31\text{-}0}$, $\text{FLAG}_{11\text{-}0}$, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTxX, DRxX, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

I = Input S = Synchronous P = Power Supply (O/D) = Open Drain
O = Output A = Asynchronous G = Ground (A/D) = Active Drive
T = Three-state (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

Pin	Type	Function
$\text{ADDR}_{23\text{-}0}$	I/O/T	**External Bus Address**. The ADSP-21065L outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of the other ADSP-21065L. The ADSP-21065L inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers.
$\text{DATA}_{31\text{-}0}$	I/O/T	**External Bus Data**. The ADSP-21065L inputs and outputs data and instructions on these pins. The external data bus transfers 32-bit single-precision floating-point data and 32-bit fixed-point data over bits 31-0. 16-bit short word data is transferred over bits 15-0 of the bus. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS}}_{3\text{-}0}$	I/O/T	**Memory Select Lines**. These lines are asserted as chip selects for the corresponding banks of external memory. Internal $\text{ADDR}_{25\text{-}24}$ are decoded into $\overline{\text{MS}}_{3\text{-}0}$. The $\overline{\text{MS}}_{3\text{-}0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{3\text{-}0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. Additionally, an $\overline{\text{MS}}_{3\text{-}0}$ line which is mapped to SDRAM may be asserted even when no SDRAM access is active. In a multiprocessor system, the $\overline{\text{MS}}_{3\text{-}0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe**. This pin is asserted when the ADSP-21065L reads from external memory devices or from the IOP register of another ADSP-21065L. External devices (including another ADSP-21065L) must assert $\overline{\text{RD}}$ to read from the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{RD}}$ is output by the bus master and is input by another ADSP-21065L.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted when the ADSP-21065L writes to external memory devices or to the IOP register of another ADSP-21065L. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{WR}}$ is output by the bus master and is input by the other ADSP-21065L.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal interfaces the ADSP-21065L to synchronous memory devices (including another ADSP-21065L). The ADSP-21065L asserts $\overline{\text{SW}}$ to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessor system, $\overline{\text{SW}}$ is output by the bus master and is input by the other ADSP-21065L to determine if the multiprocessor access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output.
ACK	I/O/S	**Memory Acknowledge**. External devices can deassert ACK to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21065L deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. In a multiprocessor system, a slave ADSP-21065L deasserts the bus master's ACK input to add wait state(s) to an access of its IOP registers. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ to place the external bus address, data, selects, and strobes—but not SDRAM control pins—in a high impedance state for the following cycle. If the ADSP-21065L attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not finish until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21065L deadlock.
$\overline{\text{IRQ}}_{2\text{-}0}$	I/A	Interrupt Request Lines. May be either edge-triggered or level-sensitive.
$\text{FLAG}_{11\text{-}0}$	I/O/A	Flag Pins. Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.

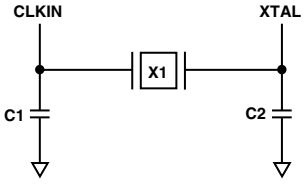
Pin	Type	Function
$\overline{HBR}$	I/A	**Host Bus Request.** Must be asserted by a host processor to request control of the ADSP-21065L's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-21065L that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-21065L places the address, data, select, and strobe lines in a high impedance state. It does, however, continue to drive the SDRAM control pins. $\overline{HBR}$ has priority over all ADSP-21065L bus requests ($\overline{BR}_{2-1}$) in a multiprocessor system.
$\overline{HBG}$	I/O	**Host Bus Grant**. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted by the ADSP-21065L until $\overline{HBR}$ is released. In a multiprocessor system, $\overline{HBG}$ is output by the ADSP-21065L bus master.
$\overline{CS}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21065L.
REDY (O/D)	O	**Host Bus Acknowledge.** The ADSP-21065L deasserts REDY to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR}_1$	I/A	**DMA Request 1** (DMA Channel 9).
$\overline{DMAR}_2$	I/A	**DMA Request 2** (DMA Channel 8).
$\overline{DMAG}_1$	O/T	**DMA Grant 1** (DMA Channel 9).
$\overline{DMAG}_2$	O/T	**DMA Grant 2** (DMA Channel 8).
$\overline{BR}_{2-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21065Ls to arbitrate for bus mastership. An ADSP-21065L drives its own $\overline{BR}$x line (corresponding to the value of its ID_{2-0} inputs) only and monitors all others. In a uniprocessor system, tie both $\overline{BR}$x pins to VDD.
ID_{1-0}	I	**Multiprocessing ID.** Determines which multiprocessor bus request ($\overline{BR}_1$–$\overline{BR}_2$) is used by ADSP-21065L. ID = 01 corresponds to $\overline{BR}_1$, ID = 10 corresponds to $\overline{BR}_2$. ID = 00 in single-processor systems. These lines are a system configuration selection which should be hard-wired or changed only at reset.
$\overline{CPA}$ (O/D)	I/O	**Core Priority Access.** Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-21065L bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open drain output that is connected to both ADSP-21065Ls in the system. The $\overline{CPA}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, leave the $\overline{CPA}$ pin unconnected.
DTxX	O	**Data Transmit** (Serial Ports 0, 1; Channels A, B). Each DTxX pin has a 50 kΩ internal pull-up resistor.
DRxX	I	**Data Receive** (Serial Ports 0, 1; Channels A, B). Each DRxX pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock** (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock** (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	**Transmit Frame Sync** (Serial Ports 0, 1).
RFSx	I/O	**Receive Frame Sync** (Serial Ports 0, 1).
BSEL	I	**EPROM Boot Select.** When BSEL is high, the ADSP-21065L is configured for booting from an 8-bit EPROM. When BSEL is low, the BSEL and $\overline{BMS}$ inputs determine booting mode. See $\overline{BMS}$ for details. This signal is a system configuration selection which should be hard-wired.

Pin	Type	Function
$\overline{\text{BMS}}$	I/O/T*	**Boot Memory Select.** Output: used as chip select for boot EPROM devices (when BSEL = 1). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. Input: When low, indicates that no booting will occur and that the ADSP-21065L will begin executing instructions from external memory. See following table. This input is a system configuration selection which should be hard-wired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). **BSEL** / **$\overline{\text{BMS}}$** / **Booting Mode** 1 / Output / EPROM (connect $\overline{\text{BMS}}$ to EPROM chip select). 0 / 1 (Input) / Host processor (HBW [SYSCON] bit selects host bus width). 0 / 0 (Input) / No booting. Processor executes from external memory.
CLKIN	I	**Clock In.** Used in conjunction with XTAL, configures the ADSP-21065L to use either its internal clock generator or an external clock source. The external crystal should be rated at 1x frequency. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. The ADSP-21065L's internal clock generator multiplies the 1x clock to generate 2x clock for its core and SDRAM. It drives 2x clock out on the SDCLKx pins for the SDRAM interface to use. See also SDCLKx. Connecting the 1x external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21065L to use the external clock source. The instruction cycle rate is equal to 2x CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-21065L to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21065L. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	**Emulation Status.** Must be connected to the ADSP-21065L EZ-ICE target board connector only.
BMSTR	O	**Bus Master Output.** In a multiprocessor system, indicates whether the ADSP-21065L is current bus master of the shared external bus. The ADSP-21065L drives BMSTR high only while it is the bus master. In a single-processor system (ID = 00), the processor drives this pin high.
$\overline{\text{CAS}}$	I/O/T	**SDRAM Column Access Strobe.** Provides the column address. In conjunction with $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{RAS}}$	I/O/T	**SDRAM Row Access Strobe.** Provides the row address. In conjunction with $\overline{\text{CAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used to block write operations.
$\text{SDCLK}_{1\text{-}0}$	I/O/S/T	**SDRAM 2x Clock Output.** In systems with multiple SDRAM devices connected in parallel, supports the corresponding increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK_1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with your SDRAM device.

Pin	Type	Function
SDA10	O/T	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a host access.
$\overline{\text{XTAL}}$	O	**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to enable the ADSP-21065L's internal clock generator or to disable it to use an external clock source. See CLKIN.
$\overline{\text{PWM_EVENT}}_{1-0}$	I/O/A	**PWM Output/Event Capture.** In PWMOUT mode, is an output pin and functions as a timer counter. In WIDTH_CNT mode, is an input pin and functions as a pulse counter/event capture.
VDD	P	**Power Supply;** nominally +3.3 V dc. (33 pins)
GND	G	**Power Supply Return**. (37 pins)
NC		**Do Not Connect.** Reserved pins that must be left open and unconnected. (7)

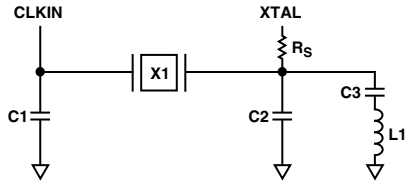
CLOCK SIGNALS

The ADSP-21065L can use an external clock or a crystal. See CLKIN pin description. You can configure the ADSP-21065L to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. You can use either a crystal operating in the fundamental mode or a crystal operating at an overtone. Figure 4 shows the component connections used for a crystal operating in fundamental mode, and Figure 5 shows the component connections used for a crystal operating at an overtone.



SUGGESTED COMPONENTS FOR 30 MHz OPERATION:
ECLIPTEK EC2SM-33-30.000M (SURFACE MOUNT PACKAGE)
ECLIPTEK EC-33-30.000M (THRU-HOLE PACKAGE)
C1 = 33pF
C2 = 27pF
NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1.
CONTACT CRYSTAL MANUFACTURER FOR DETAILS.

Figure 4. 30 MHz Operation (Fundamental Mode Crystal)



SUGGESTED COMPONENTS FOR 30MHz OPERATION:
ECLIPTEK EC2SM-T-30.000M (SURFACE MOUNT PACKAGE)
ECLIPTEK ECT-30.000M (THRU-HOLE PACKAGE)
C1 = 18pF
C2 = 27pF
C3 = 75pF
L_1 = 3300nH
R_S = SEE NOTE.
NOTE: C1, C2, C3, R_S AND L_1 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT MANUFACTURER FOR DETAILS.

Figure 5. 30 MHz Operation (3rd Overtone Crystal)

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$ and GND signals be made accessible on the target system via a 14-pin connector (a 2 row x 7 pin strip header) such as that shown in Figure 6. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you, intend to use the ADSP-2106x EZ-ICE.

The total trace length between the EZ-ICE connector and the furthest device sharing the EZ-ICE JTAG pins should be limited to 15 inches maximum for guaranteed operation. This restriction on length must include EZ-ICE JTAG signals, which are routed to one or more 2106x devices or to a combination of 2106xs and other JTAG devices on the chain.

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—you must remove Pin 3 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie and Samtec.

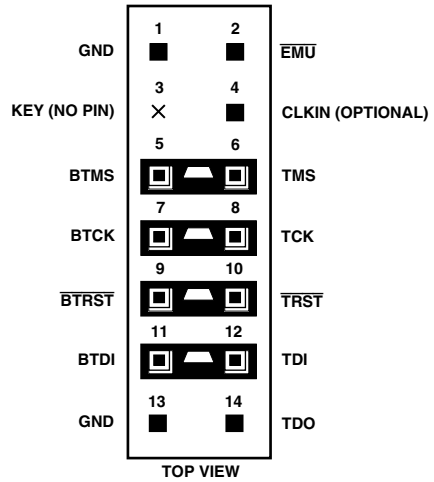


Figure 6. Target Board Connector for ADSP-2106x EZ-ICE (JTAG Header)

The BTMS, BTCK, $\overline{\text{BTRST}}$ and BTDI signals are provided so that the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the Bxxx pins and the xxx pins. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull-up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as follows:

Signal	Termination
TMS	Driven through 22 Ω resistor (16 mA driver)
TCK	Driven at 10 MHz through 22 Ω resistor (16 mA driver)
$\overline{\text{TRST}}$*	Driven through 22 Ω resistor (16 mA driver) (pulled up by on-chip 20 kΩ resistor)
TDI	Driven by 22 Ω resistor (16 mA driver)
TDO	One TTL load, Split Termination (160/220)
CLKIN	One TTL load, Split Termination (160/220). (Caution: Do not connect to CLKIN if internal XTAL oscillator is used.)
EMU	Active Low 4.7 kΩ pull-up resistor, one TTL load (open-drain output from ADSP-2106xs)

*$\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software start-up. After software start-up, $\overline{\text{TRST}}$ is driven high.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping two ADSP-21065Ls in a synchronous manner. If you do not need these operations to occur synchronously on the two processors, simply tie Pin 4 of the EZ-ICE header to ground.

For systems which use the internal clock generator and an external discrete crystal, do not directly connect the CLKIN pin to the JTAG probe. This will load the oscillator circuit and possibly cause it to fail to oscillate. Instead the JTAG probe's CLKIN can be driven by the XTAL pin through a high impedance buffer.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between multiple ADSP-2106x processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one cycle between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board.

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$ and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

For Complete information on the SHARC EZ-ICE, see the *ADSP-21000 Family JTAG EZ-ICE User's Guide and Reference.*

ADSP-21065L–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Test Conditions	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Units
V_{DD}	Supply Voltage		3.13	3.60	3.13	3.60	V
T_{CASE}	Case Operating Temperature		–40	+100	0	+85	°C
V_{IH}	High Level Input Voltage	@ V_{DD} = max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
V_{IL1}	Low Level Input Voltage[1]	@ V_{DD} = min	–0.5	0.8	–0.5	0.8	V
V_{IL2}	Low Level Input Voltage[2]	@ V_{DD} = min	–0.5	0.7	–0.5	0.7	V

NOTE
See Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	C & K Grades Min	C & K Grades Max	Units
V_{OH}	High Level Output Voltage[3]	@ V_{DD} = min, I_{OH} = –2.0 mA[4]	2.4		V
V_{OL}	Low Level Output Voltage[3]	@ V_{DD} = min, I_{OL} = 4.0 mA[4]		0.4	V
I_{IH}	High Level Input Current[5]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[5]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[6]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[7, 8, 9, 10]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V		8	µA
I_{OZLS}	Three-State Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZLA}	Three-State Leakage Current[11]	@ V_{DD} = max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}	Three-State Leakage Current[10]	@ V_{DD} = max, V_{IN} = 0 V		4	mA
I_{OZLC}	Three-State Leakage Current[9]	@ V_{DD} = max, V_{IN} = 0 V		1.5	mA
C_{IN}	Input Capacitance[12, 13]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		8	pF

NOTES
[1] Applies to input and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, BSEL, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{11-0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{2-1}$, $\overline{ID}_{2-0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0A, DR1A, DR0B, DR1B, TCLK0, TCLK1, RCLK0, RCLK1, $\overline{RESET}$, $\overline{TRST}$, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{SDCKE}$.
[2] Applies to input pin CLKIN.
[3] Applies to output and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, MS_{3-0}, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{2-1}$, $\overline{CPA}$, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, DT0A, DT1A, DT0B, DT1B, XTAL, $\overline{BMS}$, TDO, $\overline{EMU}$, BMSTR, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{DQM}$, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10.
[4] See Output Drive Currents for typical drive current capabilities.
[5] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{1-0}, BSEL, CLKIN, $\overline{RESET}$, TCK (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership.)
[6] Applies to input pins with internal pull-ups: DR0A, DR1A, DR0B, DR1B, $\overline{TRST}$, TMS, TDI.
[7] Applies to three-statable pins: $DATA_{31-0}$, $ADDR_{23-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $FLAG_{11-0}$, REDY, $\overline{HBG}$, $\overline{DMAG}_1$, $\overline{DMAG}_2$, $\overline{BMS}$, TDO, $\overline{RAS}$, $\overline{CAS}$, $\overline{DQM}$, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10 and $\overline{EMU}$ (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{1-0} = 01 and another ADSP-21065L is not requesting bus mastership).
[8] Applies to three-statable pins with internal pull-ups: DT0A, DT1A, DT0B, DT1B, TCLK0, TCLK1, RCLK0, RCLK1.
[9] Applies to $\overline{CPA}$ pin.
[10] Applies to ACK pin when pulled up.
[11] Applies to ACK pin when keeper latch enabled.
[12] Guaranteed but not tested.
[13] Applies to all signal pins.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 130°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 seconds) . . . . . +280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21065L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

POWER DISSIPATION ADSP-21065L

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note SHARC Power Dissipation Measurements.

Specifications are based on the following operating scenarios:

Table II. Internal Current Measurements

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE16 \times I_{DDIDLE16} = POWER\ CONSUMPTION$$

Table III. Internal Current Measurement Scenarios

Parameter		Test Conditions	Max	Units
$I_{DDINPEAK}$	Supply Current (Internal)[1]	t_{CK} = 33 ns, V_{DD} = max	470	mA
		t_{CK} = 30 ns, V_{DD} = max	510	mA
$I_{DDINHIGH}$	Supply Current (Internal)[2]	t_{CK} = 33 ns, V_{DD} = max	275	mA
		t_{CK} = 30 ns, V_{DD} = max	300	mA
$I_{DDINLOW}$	Supply Current (Internal)[3]	t_{CK} = 33 ns, V_{DD} = max	240	mA
		t_{CK} = 30 ns, V_{DD} = max	260	mA
I_{DDIDLE}	Supply Current (IDLE)[4]	t_{CK} = 33 ns, V_{DD} = max	150	mA
		t_{CK} = 30 ns, V_{DD} = max	155	mA
$I_{DDIDLE16}$	Supply Current (IDLE16)[5]	V_{DD} = max	50	mA

NOTES

[1]The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2]$I_{DDINHIGH}$ is a composite average based on a range of high activity code.

[3]$I_{DDINLOW}$ is a composite average based on a range of low activity code.

[4]IDLE denotes ADSP-21065L state during execution of IDLE instruction.

[5]IDLE16 denotes ADSP-21065L state during execution of IDLE16 instruction.

TIMING SPECIFICATIONS

General Notes

Two speed grades of the ADSP-21065L are offered, 60 MHz and 66 MHz instruction rates. The specifications shown are based on a CLKIN frequency of 30 MHz (t_{CK} = 33.3 ns). The DT derating allows specifications at other CLKIN frequencies (within the min–max range of the t_{CK} specification; see Clock Input below). DT is the difference between the actual CLKIN period and a CLKIN period of 33.3 ns:

$$DT = (t_{CK} - 33.3)/32$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

See Figure 27 in Equivalent Device Loading for AC Measurements (Includes All Fixtures) for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(O/D) = Open Drain
(A/D) = Active Drive

Parameter		66 MHz Min	66 MHz Max	60 MHz Min	60 MHz Max	Units
Clock Input						
Timing Requirements:						
t_{CK}	CLKIN Period	30.00	100	33.33	100	ns
t_{CKL}	CLKIN Width Low	7.0		7.0		ns
t_{CKH}	CLKIN Width High	5.0		5.0		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3.0		3.0	ns

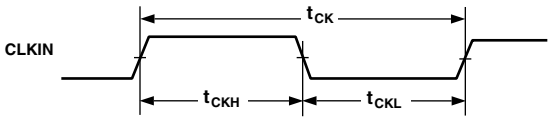


Figure 7. Clock Input

Parameter		Min	Max	Units
Reset				
Timing Requirements:				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	2 t_{CK}		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	23.5 + 24 DT	t_{CK}	ns

NOTES
[1]Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 3000 CLKIN cycles while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).
[2]Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (i.e., for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

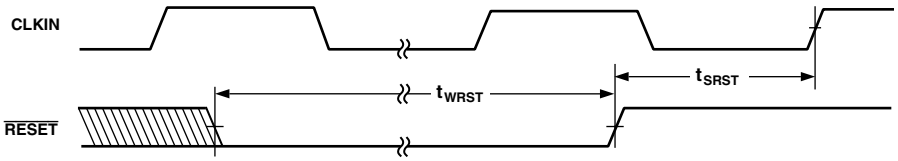


Figure 8. Reset

Parameter		Min	Max	Units
Interrupts				
Timing Requirements:				
t_{SIR}	$\overline{\text{IRQ}}$2-0 Setup Before CLKIN High or Low[1]	11.0 + 12 DT		ns
t_{HIR}	$\overline{\text{IRQ}}$2-0 Hold Before CLKIN High or Low[1]		0.0 + 12 DT	ns
t_{IPW}	$\overline{\text{IRQ}}$2-0 Pulsewidth[2]	2.0 + t_{CK}/2		ns

NOTES
[1]Only required for $\overline{\text{IRQ}}$x recognition in the following cycle.
[2]Applies only if t_{SIR} and t_{HIR} requirements are not met.

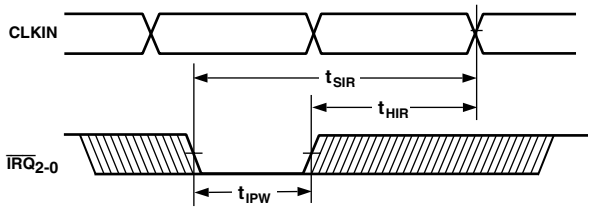


Figure 9. Interrupts

Parameter		Min	Max	Units
Timer				
Timing Requirements:				
t_{STI}	Timer Setup Before SDCLK High	0.0		ns
t_{HTI}	Timer Hold After SDCLK High	6.0		ns
Switching Characteristics:				
t_{DTEX}	Timer Delay After SDCLK High		1.0	ns
t_{HTEX}	Timer Hold After SDCLK High	–5.0		ns

Parameter		Min	Max	Units
Flags				
Timing Requirements:				
t_{SFI}	$FLAG_{11-0}$IN Setup Before SDCLK High[1]	–2.0		ns
t_{HFI}	$FLAG_{11-0}$IN Hold After SDCLK High[1]	6.0		ns
Switching Characteristics:				
t_{DFO}	$FLAG_{11-0}$OUT Delay After SDCLK High		1.0	ns
t_{HFO}	$FLAG_{11-0}$OUT Hold After SDCLK High	–4.0		ns
t_{DFOE}	SDCLK High to $FLAG_{11-0}$OUT Enable	–4.0		ns
t_{DFOD}	SDCLK High to $FLAG_{11-0}$OUT Disable		–1.75	ns

NOTE
[1]Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

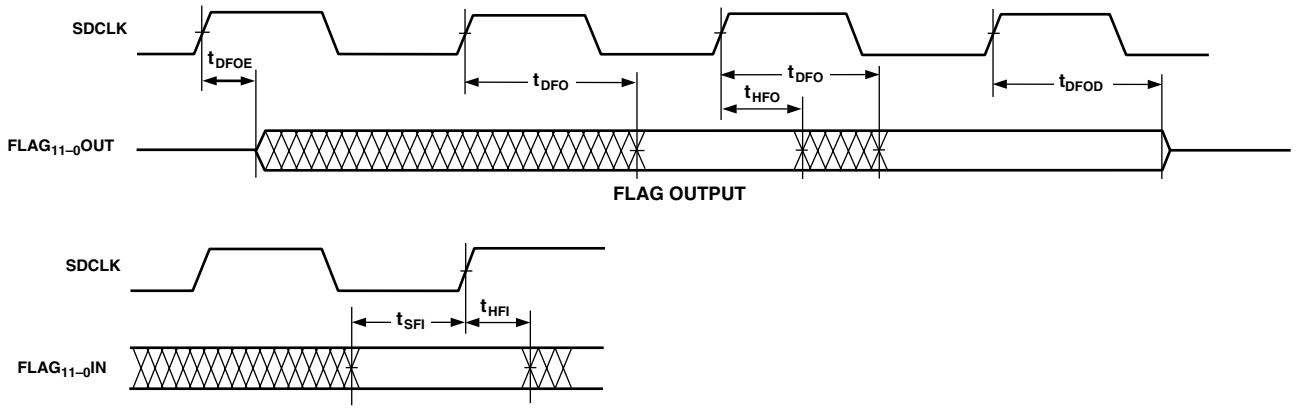


Figure 10. Flags

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21065L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write—Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa). An exception to this is the ACK pin timing requirements as described in the note below.

Parameter		Min	Max	Units
Timing Requirements:				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		28.0 + 32 DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		24.0 + 26 DT + W	ns
t_{HDA}	Data Hold from Address Selects[3]	0.0		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	0.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 3]		24.0 + 30 DT + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[3]		19.5 + 24 DT + W	ns
Switching Characteristics:				
t_{DRHA}	Address, Selects Hold After $\overline{RD}$ High	–1.0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[2]	3.0 + 6 DT		ns
t_{RW}	$\overline{RD}$ Pulsewidth	25.0 + 26 DT + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$ Low	4.5 + 6 DT + HI		ns
t_{RDGL}	$\overline{RD}$ High to $\overline{DMAG}$x Low	11.0 +12 DT + HI		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

NOTES
[1]Data Delay/Setup: User must meet t_{DAD} or to t_{DRLD} or synchronous specification t_{SSDATI}.
[2]The falling edge of $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, are referenced.
[3]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

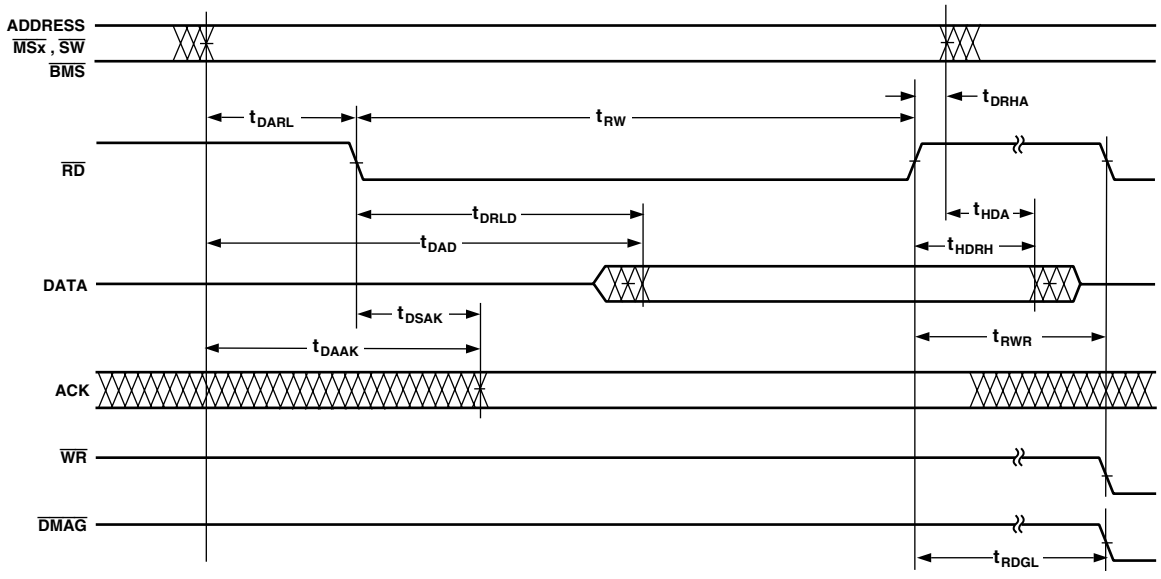


Figure 11. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21065L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write—Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa). An exception to this is the ACK pin timing requirements as described in the note below.

Parameter		Min	Max	Units
Timing Requirements:				
t_{DAAK}	ACK Delay from Address[1, 2]		24.0 + 30 DT + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		19.5 + 24 DT + W	ns
Switching Characteristics:				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	29.0 + 31 DT + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3.5 + 6 DT		ns
t_{WW}	$\overline{WR}$ Pulsewidth	24.5 + 25 DT + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	15.5 + 19 DT + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	0.0 + 1 DT + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1.0 + 1 DT + H	4.0 + 1 DT + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	4.5 + 7 DT + H		ns
t_{WRDGL}	$\overline{WR}$ High to $\overline{DMAG}$x Low	11.0 + 13 DT + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	3.5 + 6 DT + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	4.5 + 6 DT		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

NOTES

[1]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[2]The falling edge of $\overline{MS}$x, $\overline{SW}$, and $\overline{BMS}$ is referenced.

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

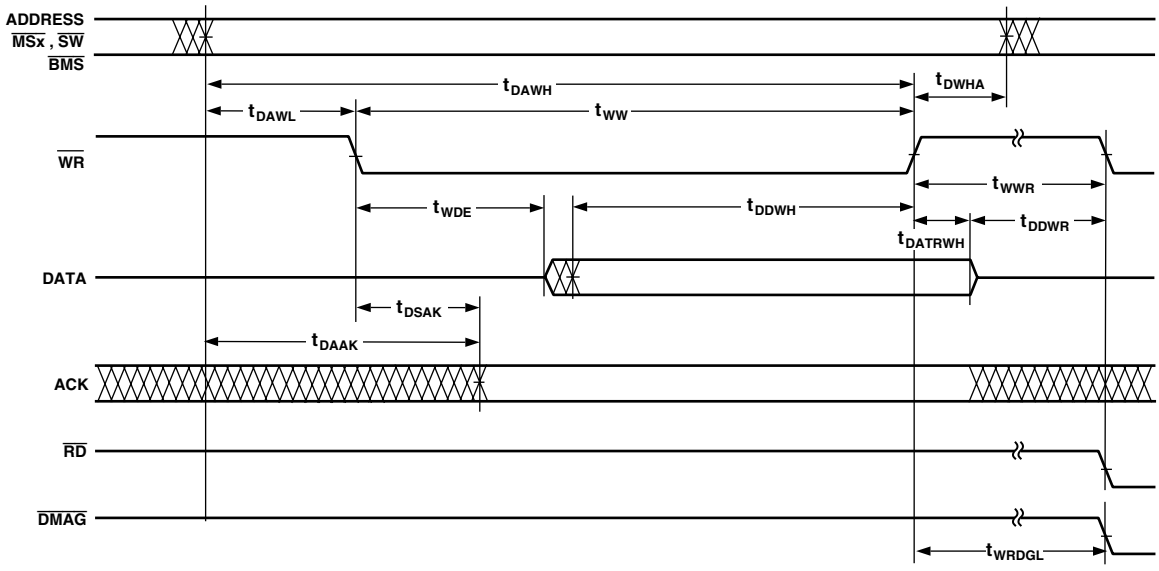


Figure 12. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN-relative timing or for accessing a slave ADSP-21065L (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see Memory Read—Bus Master and Memory Write—Bus Master).

When accessing a slave ADSP-21065L, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave). The slave ADSP-21065L must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		Min	Max	Units
Timing Requirements:				
t_{SSDATI}	Data Setup Before CLKIN	0.25 + 2 DT		ns
t_{HSDATI}	Data Hold After CLKIN	4.0 – 2 DT		ns
t_{DAAK}	ACK Delay After Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		24.0 + 30 DT + W	ns
t_{SACKC}	ACK Setup Before CLKIN[1]	2.75 + 4 DT		ns
t_{HACK}	ACK Hold After CLKIN	2.0 – 4 DT		ns
Switching Characteristics:				
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1]		7.0 – 2 DT	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	0.5 – 2 DT		ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	0.5 – 2 DT	6.0 – 2 DT	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	0.0 – 3 DT	6.0 – 3 DT	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	7.5 + 4 DT	11.75 + 4 DT	ns
t_{DDATO}	Data Delay After CLKIN		22.0 + 10 DT	ns
t_{DATTR}	Data Disable After CLKIN[3]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DBM}	BMSTR Delay After CLKIN		3.0	ns
t_{HBM}	BMSTR Hold After CLKIN	–4.0		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

NOTES

[1]Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification t_{HDATI}. See system hold time calculation under test conditions for the calculation of hold times given capacitive and dc loads.

[2]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

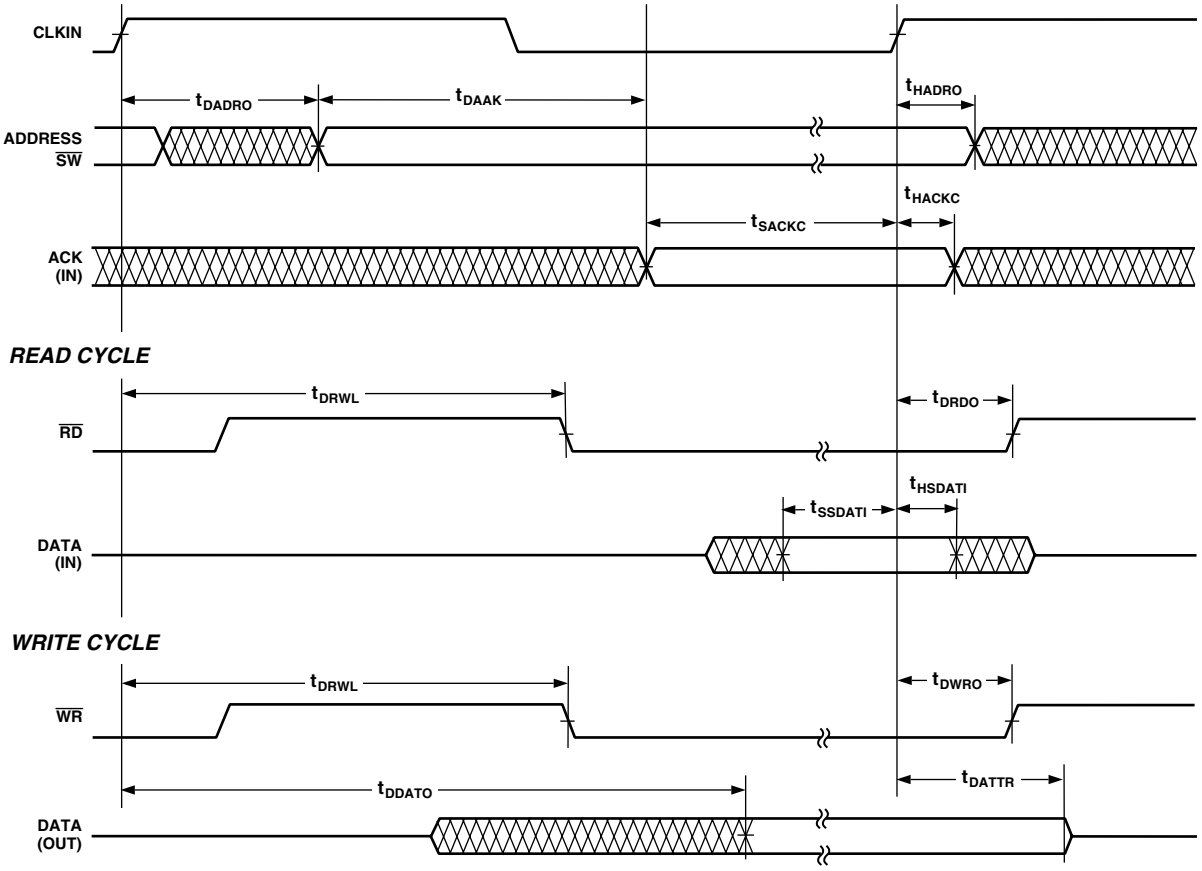


Figure 13. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for ADSP-21065L bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		Min	Max	Units
Timing Requirements:				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	24.5 + 25 DT		ns
t_{HADRI}	Address, $\overline{SW}$ Hold Before CLKIN		4.0 + 8 DT	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup Before CLKIN[1]	21.0 + 21 DT		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold After CLKIN	–2.50 – 5 DT	7.5 + 7 DT	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	2.5		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	4.5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	0.0		ns
Switching Characteristics:				
t_{SDDATO}	Data Delay After CLKIN		31.75 + 21 DT	ns
t_{DATTR}	Data Disable After CLKIN[2]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{DACK}	ACK Delay After CLKIN		29.5 + 20 DT	ns
t_{ACKTR}	ACK Disable After CLKIN[2]	1.0 – 2 DT	6.0 – 2 DT	ns

NOTES

[1]t_{SRWLI} is specified when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 17.5 + 18 DT.

[2]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

For two ADSP-21065Ls to communicate synchronously as master and slave, certain master and slave specification combinations must be satisfied. Do not compare specification values directly to calculate master/slave clock skew margins for those specifications listed below. The following table shows the appropriate clock skew margin.

Table IV. Bus Master to Slave Skew Margins

Master Specification	Slave Specification	Skew Margin	
t_{SSDATI}	t_{SDDATO}	t_{CK} = 33.3 ns	+ 2.25 ns
		t_{CK} = 30.0 ns	+ 1.50 ns
t_{SACKC}	t_{DACK}	t_{CK} = 33.3 ns	+ 3.00 ns
		t_{CK} = 30.0 ns	+ 2.25 ns
t_{DADRO}	t_{SADRI}	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	+ 2.75 ns
t_{DRWL} (Max)	t_{SRWLI}	t_{CK} = 33.3 ns	+ 1.50 ns
		t_{CK} = 30.0 ns	+ 1.25 ns
t_{DRDO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.00 ns
t_{DWRO} (Max)	t_{HRWLI} (Max)	t_{CK} = 33.3 ns	N/A
		t_{CK} = 30.0 ns	3.75 ns

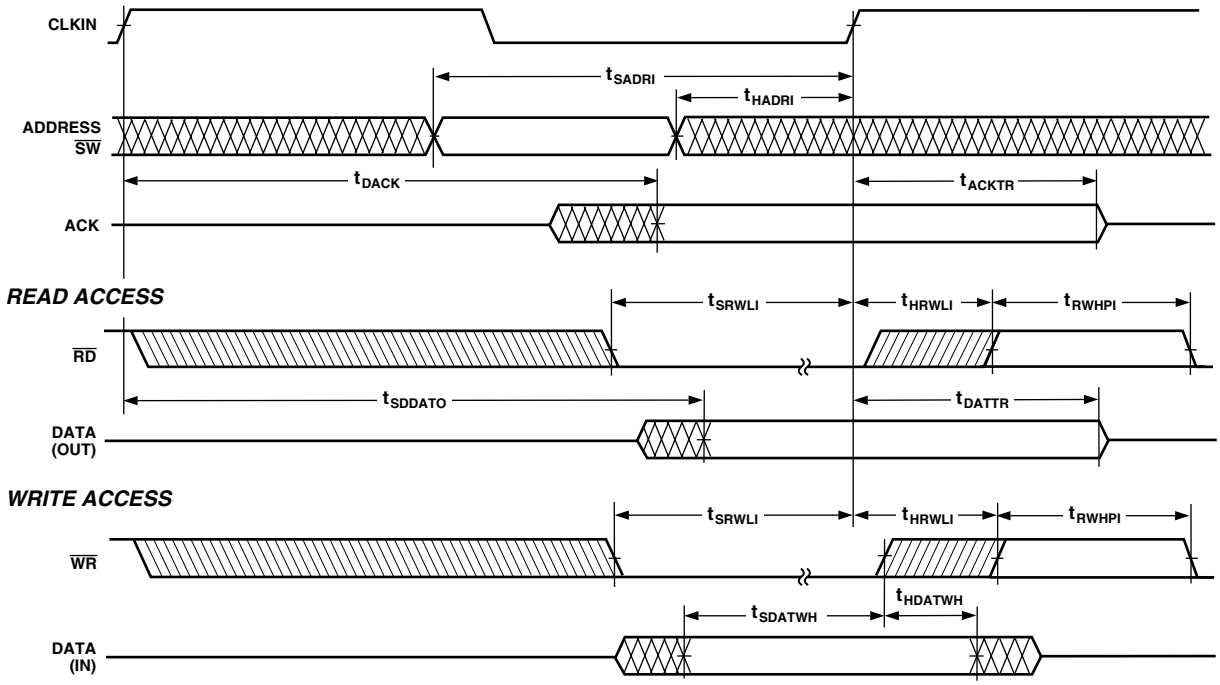


Figure 14. Synchronous Read/Write—Bus Slave

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21065Ls ($\overline{BR}$x) or a host processor ($\overline{HBR}$, $\overline{HBG}$).

Parameter		Min	Max	Units
Timing Requirements:				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		20.0 + 36 DT	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	12.0 + 12 DT		ns
t_{HHBRI}	$\overline{HBR}$ Hold Before CLKIN[2]		6.0 + 12 DT	ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	6.0 + 8 DT		ns
t_{HHBGI}	$\overline{HBG}$ Hold Before CLKIN High		1.0 + 8 DT	ns
t_{SBRI}	$\overline{BR}$x, $\overline{CPA}$ Setup Before CLKIN[3]	7.0 + 8 DT		ns
t_{HBRI}	$\overline{BR}$x, $\overline{CPA}$ Hold Before CLKIN High		1.0 + 8 DT	ns
Switching Characteristics:				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		8.0 – 2 DT	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	1.0 – 2 DT		ns
t_{DBRO}	$\overline{BR}$x Delay After CLKIN		7.0 – 2 DT	ns
t_{HBRO}	$\overline{BR}$x Hold After CLKIN	1.0 – 2 DT		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay After CLKIN		11.5 – 2 DT	ns
t_{TRCPA}	$\overline{CPA}$ Disable After CLKIN	1.0 – 2 DT	5.5 – 2 DT	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[4]		13.0	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[4]	44.0 + 43 DT		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[4]		10.0	ns

NOTES

[1]For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, $ADDR_{23-0}$ must be a nonMMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the Host Processor Control of the ADSP-21065L section of the *ADSP-21065L SHARC User's Manual*, Second Edition.

[2]Only required for recognition in the current cycle.

[3]$\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

[4](O/D) = open drain, (A/D) = active drive.

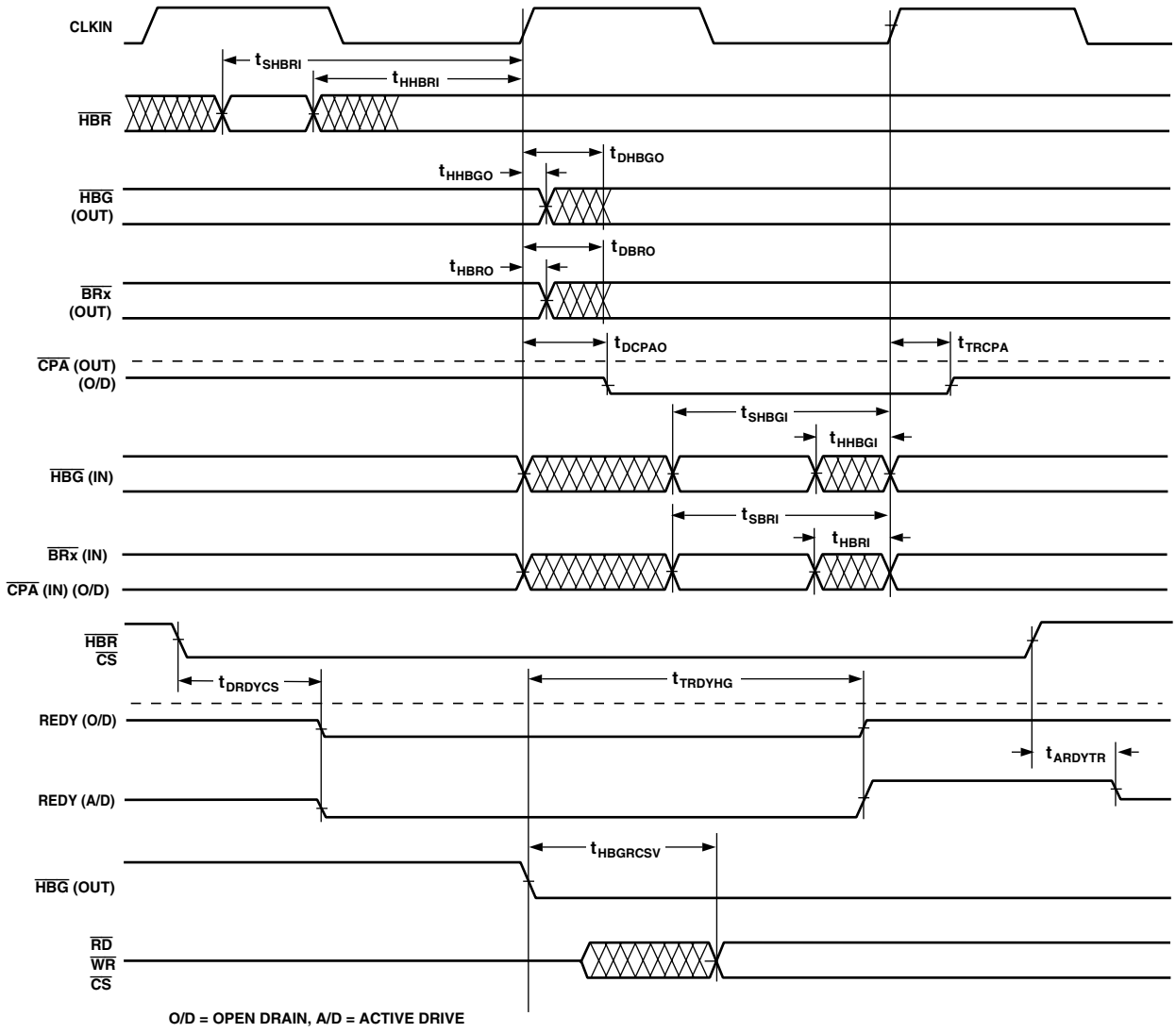


Figure 15. Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write—Host to ADSP-21065L

Use these specifications for asynchronous host processor accesses of an ADSP-21065L, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After the ADSP-21065L returns $\overline{HBG}$, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21065L's IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing. Writes can occur at a minimum interval of (1/2) t_{CK}.

Parameter		Min	Max	Units
Read Cycle				
Timing Requirements:				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low*	0.0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$ High	0.0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6.0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0.0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0.0		ns
Switching Characteristics:				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	1.5		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low		13.5	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	28.0 + DT		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2.0	10.0	ns
Write Cycle				
Timing Requirements:				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0.0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0.0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5.0		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2.0		ns
t_{WWRL}	$\overline{WR}$ Low Width	7.0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6.0		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0.0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5.0		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1.0		ns
Switching Characteristics:				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low		13.5	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write	7.75		ns

NOTE

*Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR23-0 must be a nonMMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See Host Interface, in the *ADSP-21065L SHARC User's Manual*, Second Edition.

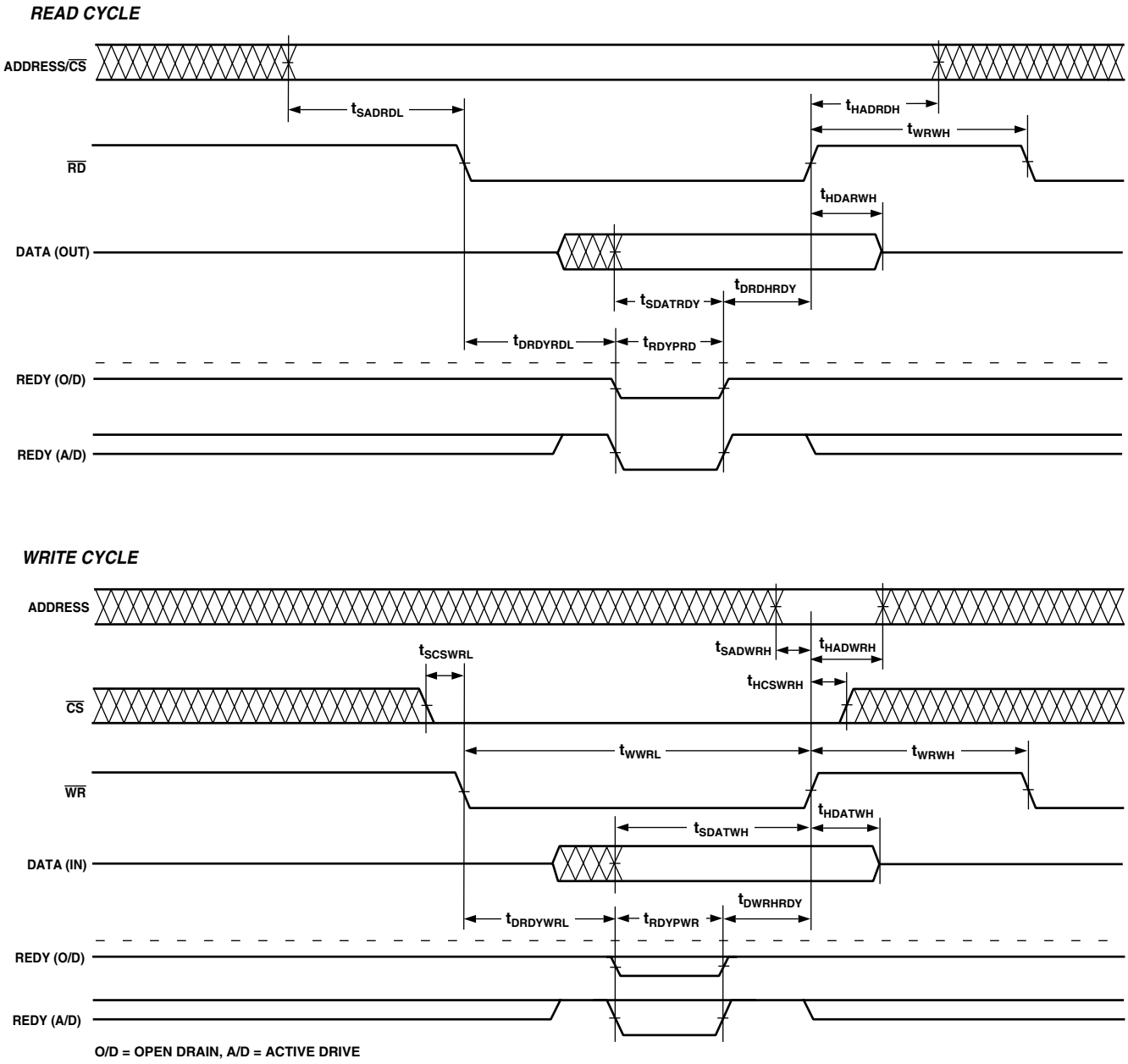


Figure 16. Asynchronous Read/Write—Host to ADSP-21065L

Three-State Timing—Bus Master, Bus Slave, $\overline{\text{HBR}}$, $\overline{\text{SBTS}}$

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Parameter		Min	Max	Units
Timing Requirements:				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	7.0 + 8 DT		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold Before CLKIN		1.0 + 8 DT	ns
Switching Characteristics:				
t_{MIENA}	Address/Select Enable After CLKIN	1.0 – 2 DT		ns
t_{MIENS}	Strobes Enable After CLKIN[1]	–0.5 – 2 DT		ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	2.0 – 2 DT		ns
t_{MITRA}	Address/Select Disable After CLKIN		3.0 – 4 DT	ns
t_{MITRS}	Strobes Disable After CLKIN[1]		4.0 – 4 DT	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN		5.5 – 4 DT	ns
t_{DATEN}	Data Enable After CLKIN[2]	10.0 + 5 DT		ns
t_{DATTR}	Data Disable After CLKIN[2]	1.0 – 2 DT	7.0 – 2 DT	ns
t_{ACKEN}	ACK Enable After CLKIN[2]	7.5 + 4 DT		ns
t_{ACKTR}	ACK Disable After CLKIN[2]	1.0 – 2 DT	6.0 – 2 DT	ns
t_{MTRHBG}	Memory Interface Disable Before $\overline{\text{HBG}}$ Low[3]	2.0 + 2 DT		ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[3]	15.75 + DT		ns

NOTES

[1]Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, $\overline{\text{DMAG}}$.

[2]In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.

[3]Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}$x, $\overline{\text{SW}}$, $\overline{\text{DMAG}}$x, $\overline{\text{BMS}}$ (in EPROM boot mode).

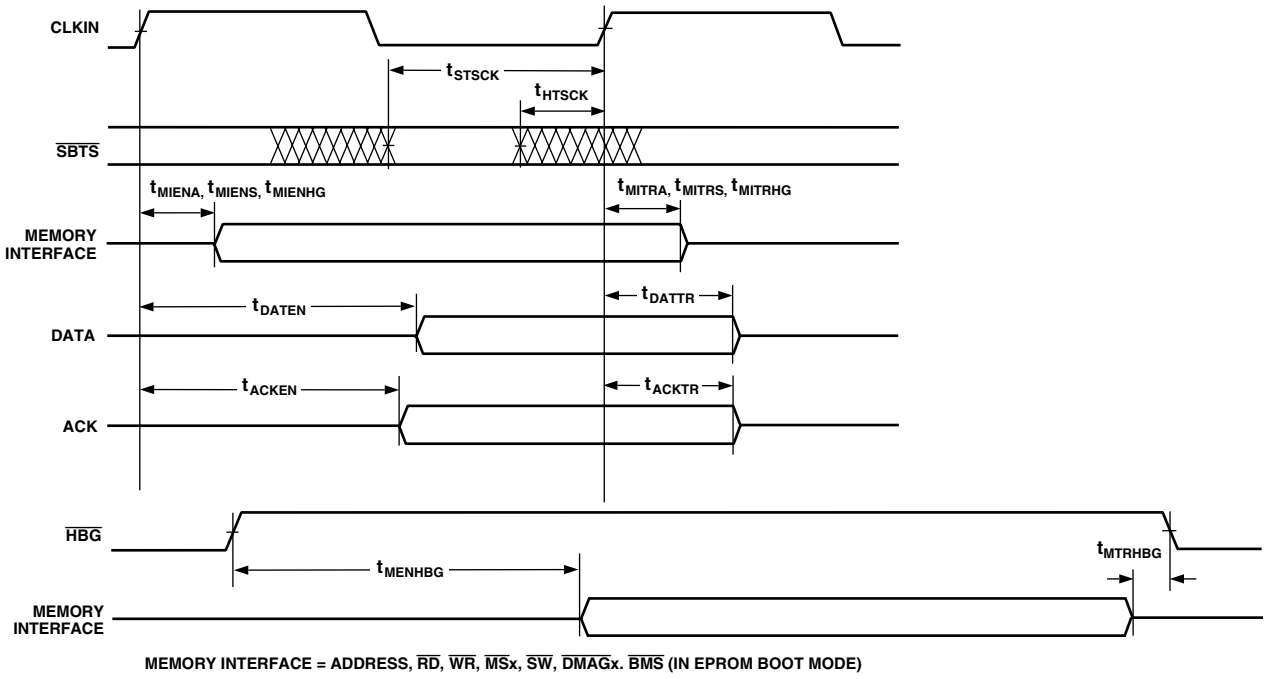


Figure 17. Three-State Timing

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes DMAR is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, $\overline{MS}_{3-0}$, ACK, and $\overline{\text{DMAG}}$ signals. Extern mode cannot be used for transfers with SDRAM. For Paced Master mode, the data transfer is controlled by $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{MS}_{3-0}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{MS}_{3-0}$, $\overline{SW}$, $DATA_{31-0}$, and ACK also apply.

Parameter		Min	Max	Units
Timing Requirements:				
t_{SDRLC}	$\overline{\text{DMAR}}$x Low Setup Before CLKIN[1]	5.0		ns
t_{SDRHC}	$\overline{\text{DMAR}}$x High Setup Before CLKIN[1]	5.0		ns
t_{WDR}	$\overline{\text{DMAR}}$x Width Low (Nonsynchronous)	6.0		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAG}}$x Low[2]		15.0 + 20 DT	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAG}}$x High	0.0		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMAR}}$x High[2]		25.0 + 14 DT	ns
t_{DMARLL}	$\overline{\text{DMAR}}$x Low Edge to Low Edge	18.0 + 14 DT		ns
t_{DMARH}	$\overline{\text{DMAR}}$x Width High	6.0		ns
Switching Characteristics:				
t_{DDGL}	$\overline{\text{DMAG}}$x Low Delay After CLKIN	14.0 + 10 DT	20.0 + 10 DT	ns
t_{WDGH}	$\overline{\text{DMAG}}$x High Width	10.0 + 12 DT + HI		ns
t_{WDGL}	$\overline{\text{DMAG}}$x Low Width	16.0 + 20 DT		ns
t_{HDGC}	$\overline{\text{DMAG}}$x High Delay After CLKIN	0.0 – 2 DT	6.0 – 2 DT	ns
t_{DADGH}	Address Select Valid to $\overline{\text{DMAG}}$x High	28.0 + 16 DT		ns
t_{DDGHA}	Address Select Hold After $\overline{\text{DMAG}}$x High	–1.0		ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAG}}$x High[3]	16.0 + 20 DT		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAG}}$x High[4]	0.0	4.0	ns
t_{DGWRL}	$\overline{WR}$ Low Before $\overline{\text{DMAG}}$x Low	5.0 + 6 DT	8.0 + 6 DT	ns
t_{DGWRH}	$\overline{\text{DMAG}}$x Low Before $\overline{WR}$ High	18.0 + 19 DT + W		ns
t_{DGWRR}	$\overline{WR}$ High Before $\overline{\text{DMAG}}$x High	0.75 + 1 DT	3.0 + 1 DT	ns
t_{DGRDL}	$\overline{RD}$ Low Before $\overline{\text{DMAG}}$x Low	5.0	8.0	ns
t_{DRDGH}	$\overline{RD}$ Low Before $\overline{\text{DMAG}}$x High	24.0 + 26 DT + W		ns
t_{DGRDR}	$\overline{RD}$ High Before $\overline{\text{DMAG}}$x High	0.0	2.0	ns
t_{DGWR}	$\overline{\text{DMAG}}$x High to $\overline{WR}$, $\overline{RD}$ Low	5.0 + 6 DT + HI		ns

W = (number of wait states specified in WAIT register) × t_{CK}.

HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

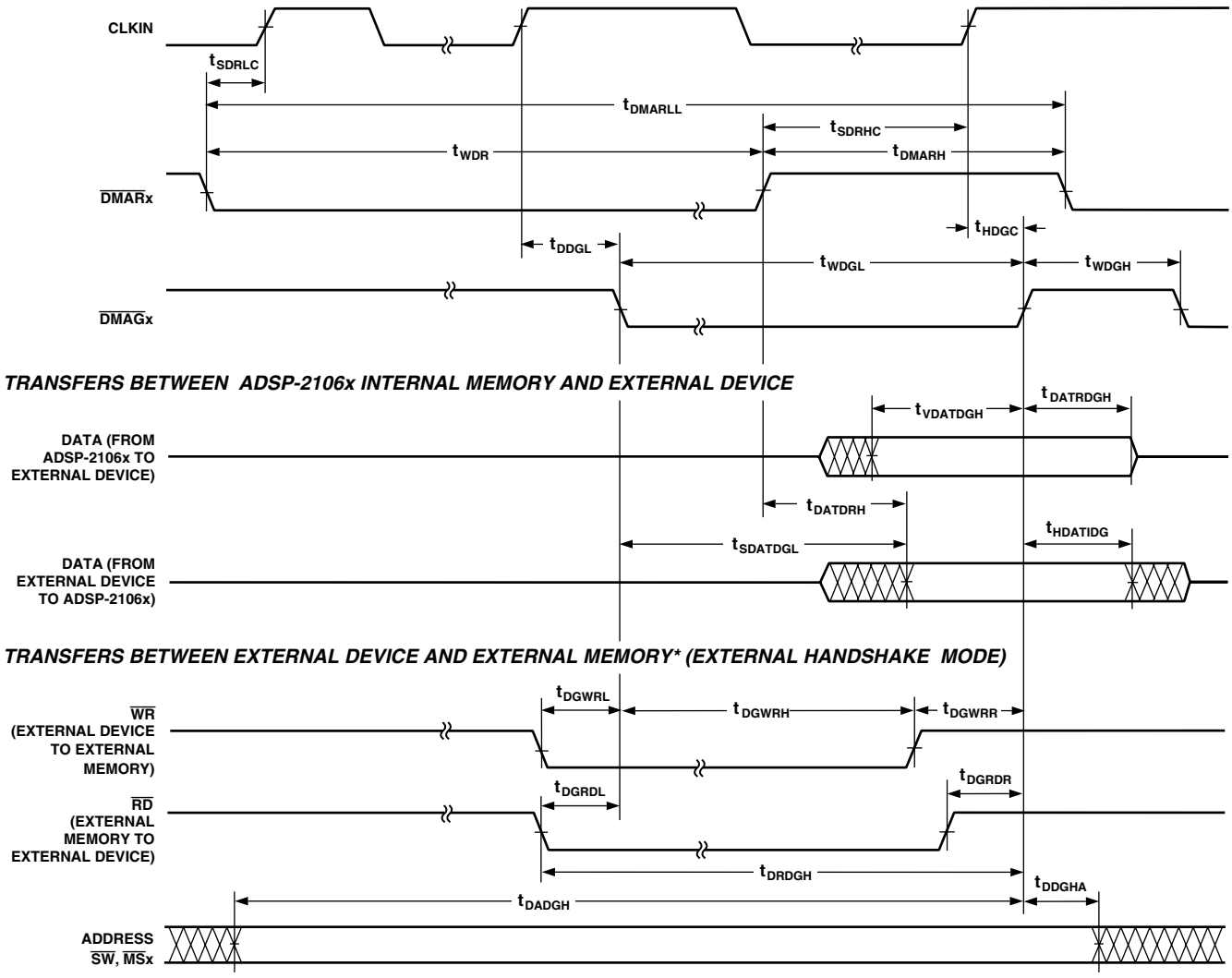
NOTES

[1]Only required for recognition in the current cycle.

[2]$t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMAR}}$x is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMAR}}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMAR}}$x is brought high.

[3]$t_{VDATDGH}$ is valid if $\overline{\text{DMAR}}$x is not being used to hold off completion of a read. If $\overline{\text{DMAR}}$x is used to prolong the read, then $t_{VDATDGH}$ = 8 + 9 DT + (n × t_{CK}) where *n* equals the number of extra cycles that the access is prolonged.

[4]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.



*"MEMORY READ – BUS MASTER," "MEMORY WRITE – BUS MASTER" AND "SYNCHRONOUS READ/WRITE – BUS MASTER" TIMING SPECIFICATIONS FOR $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, $\overline{MS}_{3-0}$ AND ACK ALSO APPLY HERE.

Figure 18. DMA Handshake Timing

SDRAM Interface—Bus Master
Use these specifications for ADSP-21065L bus master accesses of SDRAM.

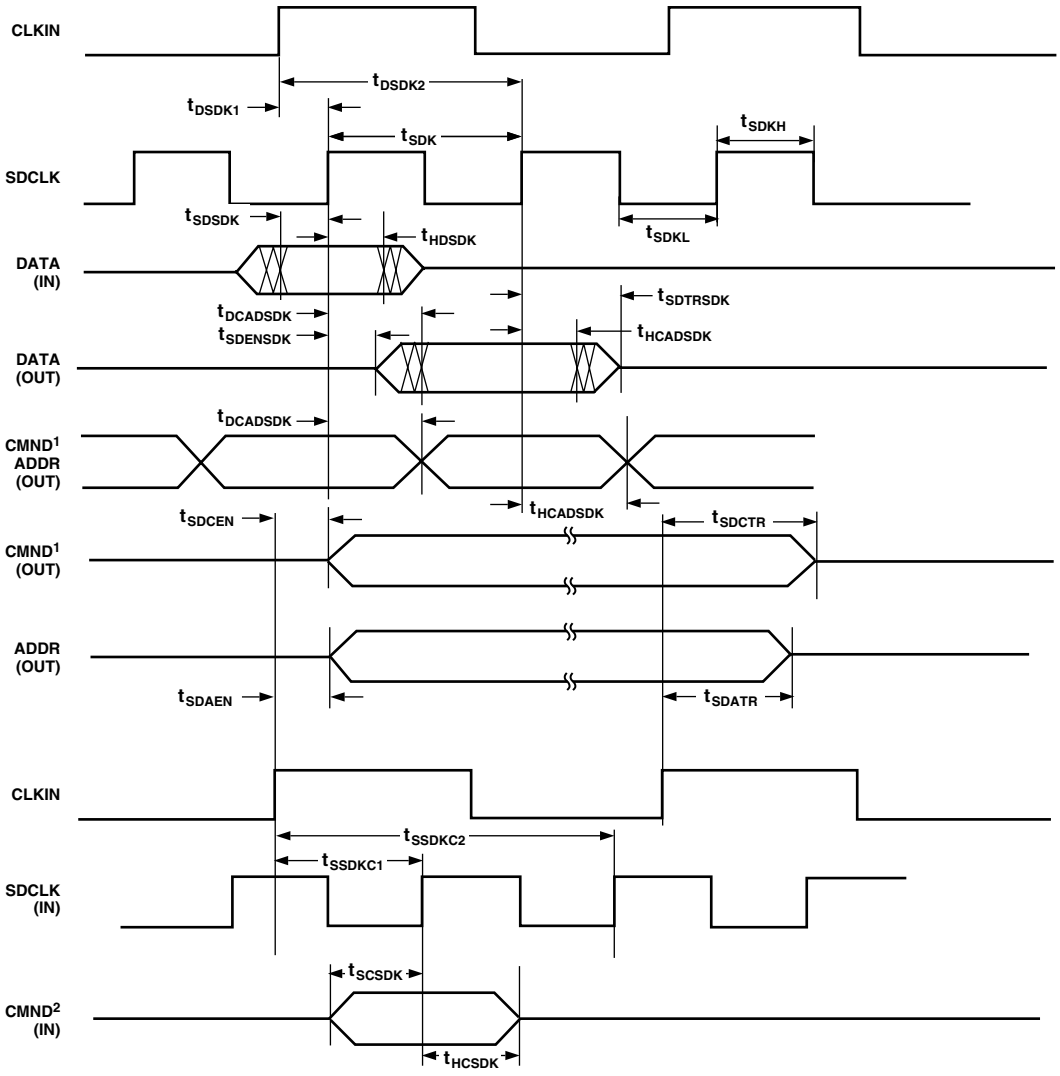
Parameter		Min	Max	Units
Timing Requirements:				
t_{SDSDK}	Data Setup Before SDCLK	2.0		ns
t_{HDSDK}	Data Hold After SDCLK	1.25		ns
Switching Characteristics:				
t_{DSDK1}	First SDCLK Rise Delay After CLKIN	9.0 + 6 DT	12.75 + 6 DT	ns
t_{DSDK2}	Second SDCLK Rise Delay After CLKIN	25.5 + 22 DT	29.25 + 22 DT	ns
t_{SDK}	SDCLK Period	16.67	$t_{CK}/2$	ns
t_{SDKH}	SDCLK Width High	7.5 + 8 DT		ns
t_{SDKL}	SDCLK Width Low	6.5 + 8 DT		ns
$t_{DCADSDK}$	Command, Address, Data, Delay After SDCLK[1]		10.0 + 5 DT	ns
$t_{HCADSDK}$	Command, Address, Data, Hold After SDCLK[1]	4.5 + 5 DT		ns
$t_{SDTRSDK}$	Data Three-State After SDCLK		9.5 + 5 DT	ns
$t_{SDENSDK}$	Data Enable After SDCLK[2]	6.0 + 5 DT		ns
t_{SDCTR}	SDCLK, Command Three-State After CLKIN[1]	5.0 + 3 DT	9.75 + 3 DT	ns
t_{SDCEN}	SDCLK, Command Enable After CLKIN[1]	5.0 + 2 DT	10.0 + 2 DT	ns
t_{SDATR}	Address Three-State After CLKIN	–1.0 – 4 DT	3.0 – 4 DT	ns
t_{SDAEN}	Address Enable After CLKIN	1.0 – 2 DT	7.0 – 2 DT	ns

NOTES
[1]Command = SDCKE, $\overline{MS}$x, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{DQM}$, and SDA10.
[2]SDRAM controller adds one SDRAM CLK three-stated cycle delay ($t_{CK}/2$) on a Read followed by a Write.

SDRAM Interface—Bus Slave
These timing requirements allow a bus slave to sample the bus master's SDRAM command and detect when a refresh occurs.

Parameter		Min	Max	Units
Timing Requirements:				
t_{SSDKC1}	First SDCLK Rise After CLKIN	6.50 + 16 DT	17.5 + 16 DT	ns
t_{SSDKC2}	Second SDCLK Rise After CLKIN	23.25	34.25	ns
t_{SCSDK}	Command Setup Before SDCLK[1]	0.0		ns
t_{HCSDK}	Command Hold After SDCLK[1]	2.0		ns

NOTE
[1]Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.



NOTES
[1]COMMAND = SDCKE, $\overline{MS_X}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{DQM}$ AND SDA10.
[2]SDRAM CONTROLLER ADDS ONE SDRAM CLK THREE-STATED CYCLE DELAY ($t_{CK}/2$) ON A READ FOLLOWED BY A WRITE.

Figure 19. SDRAM Interface

Serial Ports

Parameter		Min	Max	Units
External Clock				
Timing Requirements:				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	4.0		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1]	4.0		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4.0		ns
t_{SCLKW}	TCLK/RCLK Width	9.0		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns
Internal Clock				
Timing Requirements:				
t_{SFSI}	TFS Setup Before TCLK[2]; RFS Setup Before RCLK[1]	8.0		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1]	1.0		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3.0		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3.0		ns
External or Internal Clock				
Switching Characteristics:				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[2]		13.0	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[2]	3.0		ns
External Clock				
Switching Characteristics:				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[2]		13.0	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[2]	3.0		ns
t_{DDTE}	Transmit Data Delay After TCLK[2]		12.5	ns
t_{HDTE}	Transmit Data Hold After TCLK[2]	4.0		ns
Internal Clock				
Switching Characteristics:				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[2]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[2]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[2]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[2]	0.0		ns
t_{SCLKIW}	TCLK/RCLK Width	$(t_{SCLK}/2) - 2.5$	$(t_{SCLK}/2) + 2.5$	ns
Enable and Three-State				
Switching Characteristics:				
t_{DTENE}	Data Enable from External TCLK[2]	5.0		ns
t_{DDTTE}	Data Disable from External RCLK[2]		10.0	ns
t_{DTENI}	Data Enable from Internal TCLK[2]	0.0		ns
t_{DDTTI}	Data Disable from Internal TCLK[2]		3.0	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		18.0 + 6 DT	ns
t_{DPTR}	SPORT Disable After CLKIN		14.0	ns
External Late Frame Sync				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		10.5	ns
$t_{DTENLFSE}$	Data Enable from late FS or MCE = 1, MFD = 0[3, 4]	3.5		ns
$t_{DDTLSCK}$	Data Delay from TCLK/RCLK for Late External TFS or External RFS with MCE = 1, MFD = 0[3, 4]		12.0	ns
$t_{DTENLSCK}$	Data Enable from RCLK/TCLK for Late External FS or MCE = 1, MFD = 0[3, 4]	4.5		ns

NOTES

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup-and-hold, 2) data delay and data setup-and-hold, and 3) SCLK width.

[1]Referenced to sample edge.

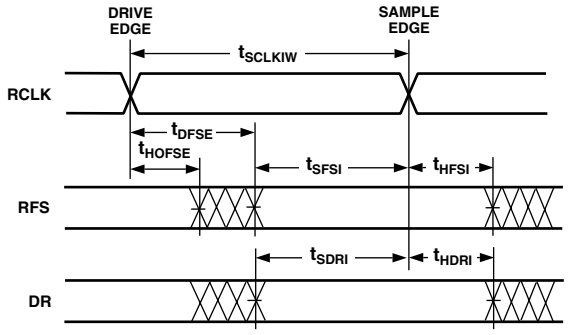
[2]Referenced to drive edge.

[3]MCE = 1, TFS enable and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.

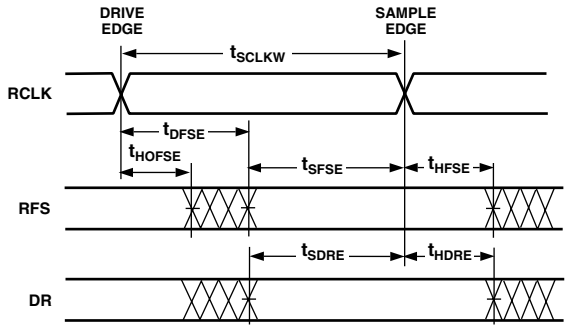
[4]If external RFS/TFS setup to RCLK/TCLK > $t_{SCLK}/2$ then $t_{DDTLSCK}$ and $t_{DTENLSCK}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

*Word selected timing for I^2S mode is the same as TFS/RFS timing (normal framing only).

DATA RECEIVE– INTERNAL CLOCK

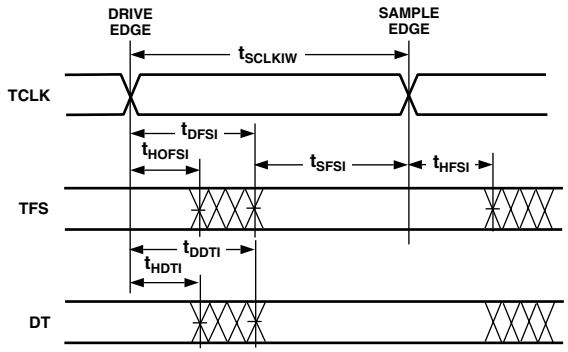


DATA RECEIVE– EXTERNAL CLOCK

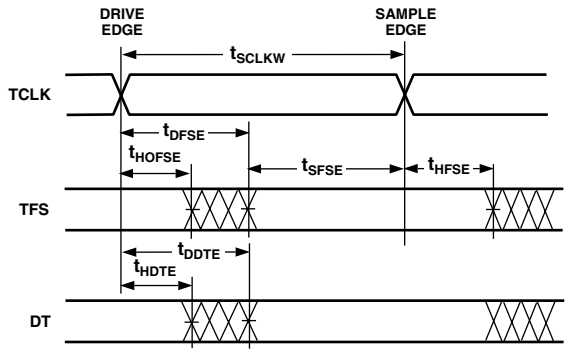


NOTE: EITHER THE RISING EDGE OR FALLING EDGE OF RCLK, TCLK CAN BE USED AS THE ACTIVE SAMPLING EDGE.

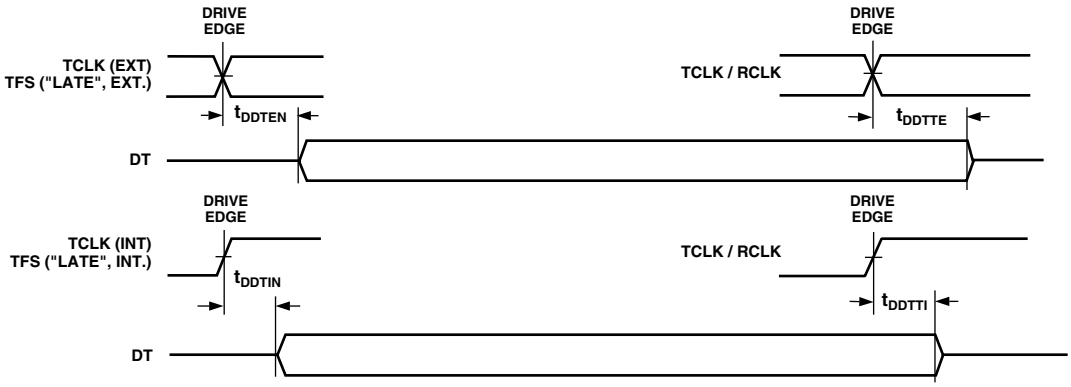
DATA TRANSMIT– INTERNAL CLOCK



DATA TRANSMIT– EXTERNAL CLOCK



NOTE: EITHER THE RISING EDGE OR FALLING EDGE OF RCLK OR TCLK CAN BE USED AS THE ACTIVE SAMPLING EDGE.



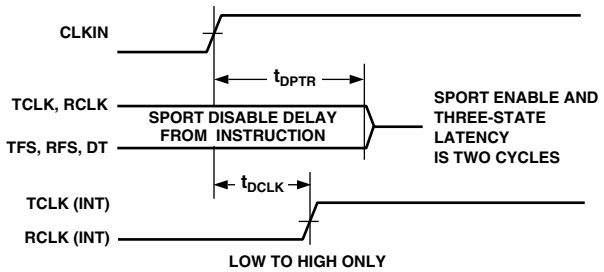


Figure 20. Serial Ports

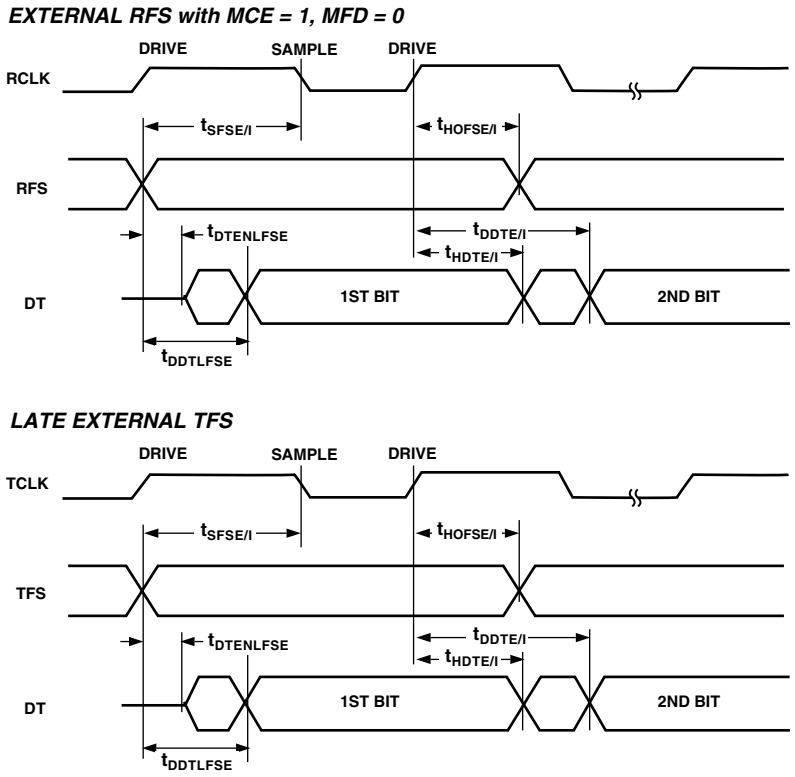


Figure 21. External Late Frame Sync (Frame Sync Setup < $t_{SCLK}/2$)

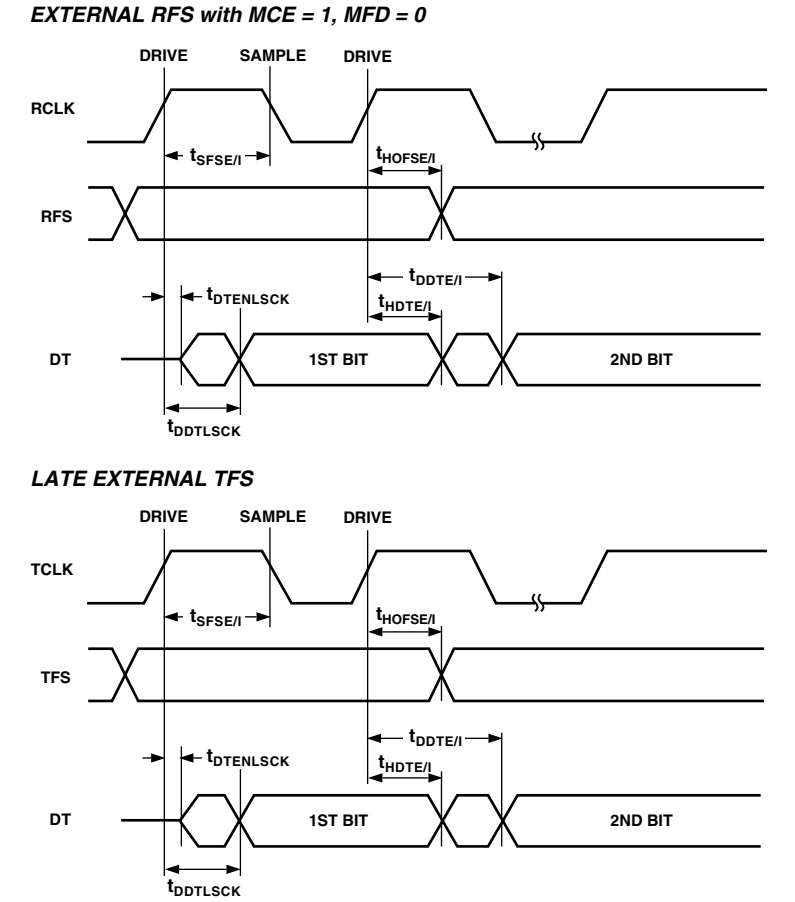


Figure 22. External Late Frame Sync (Frame Sync Setup > $t_{SCLK}/2$)

JTAG Test Access Port and Emulation

Parameter		Min	Max	Units
Timing Requirements:				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	3.0		ns
t_{HTAP}	TDI, TMS Hold After TCK High	3.0		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7.0		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	12.0		ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth	4 t_{CK}		ns
Switching Characteristics:				
t_{DTDO}	TDO Delay from TCK Low		11.0	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		15.0	ns

NOTES
[1]System Inputs = $DATA_{31-0}$, $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR_1}$, $\overline{DMAR_2}$, $\overline{BR}_{2-1}$, ID_{1-0}, $\overline{IRQ}_{2-0}$, $FLAG_{11-0}$, DR0x, DR1x, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, BSEL, $\overline{BMS}$, CLKIN, $\overline{RESET}$, $SDCLK_0$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCKE, PWM_EVENTx.
[2]System Outputs = $DATA_{31-0}$, $ADDR_{23-0}$, MS_{3-0}, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SW}$, $\overline{HBG}$, REDY, DMAG1, DMAG2, $\overline{BR}_{2-1}$, $\overline{CPA}$, $FLAG_{11-0}$, PWM_EVENTx, DT0x, DT1x, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, SDCLK0, SDCLK1, $\overline{DQM}$, SDA10, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCKE, BM, XTAL.

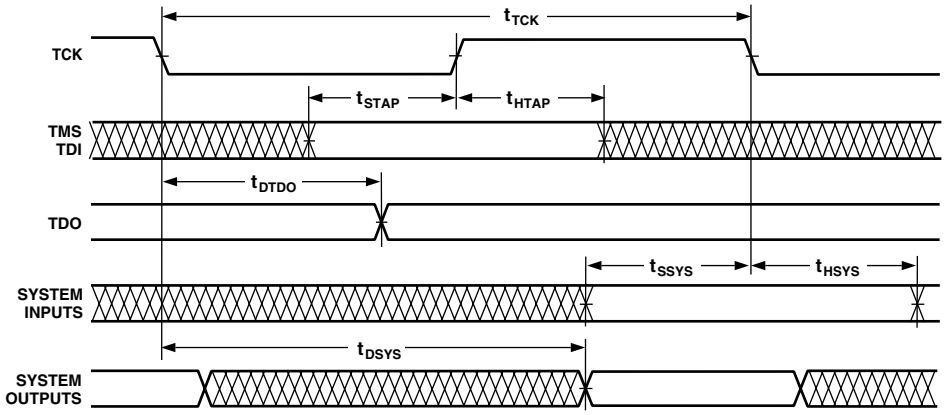


Figure 23. JTAG Test Access Port and Emulation

OUTPUT DRIVE CURRENT

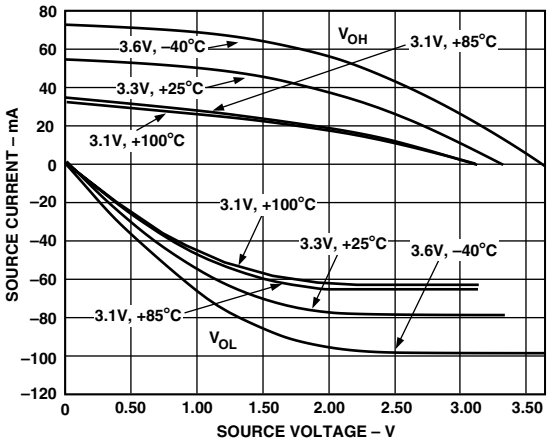


Figure 24. Typical Drive Currents

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 26. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21065L's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

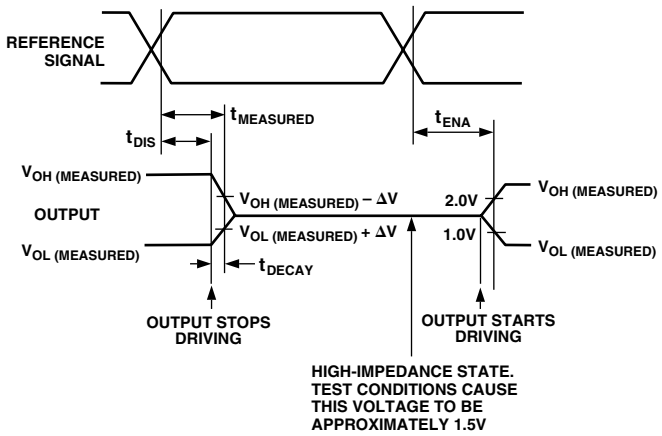


Figure 25. Output Enable

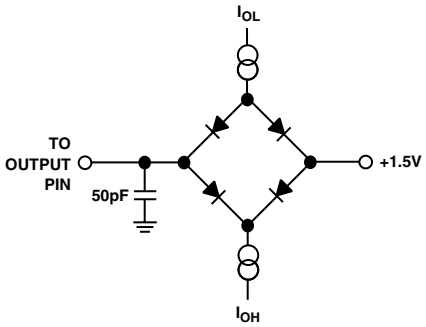


Figure 26. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

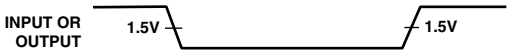


Figure 27. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins. The delay and hold specifications given should be derated by a factor of l.8 ns/50 pF for loads other than the nominal value of 50 pF. Figure 28 and Figure 29 show how output rise time varies with capacitance. Figure 30 shows graphically how output delays and hold vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable time under Test Conditions.) The graphs of Figure 28, Figure 29 and Figure 30 may not be linear outside the ranges shown.

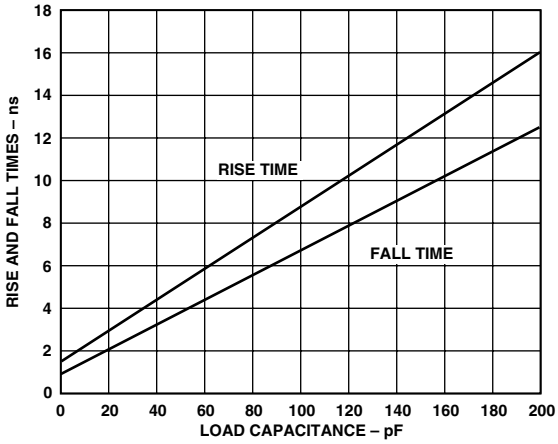


Figure 28. Typical Rise and Fall Time (10%–90% V_{DD})

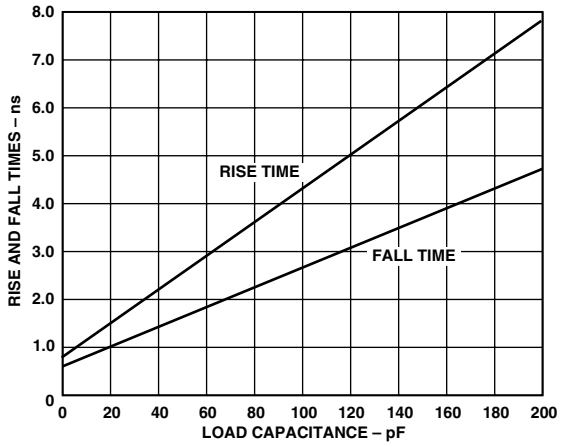


Figure 29. Typical Rise and Fall Time (0.8 V–2.0 V)

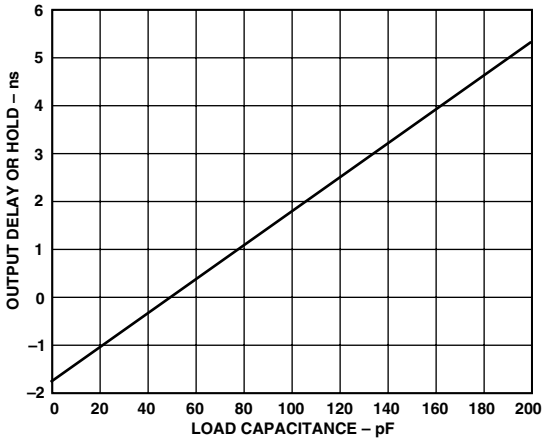


Figure 30. Typical Output Delay or Hold

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation depends on the sequence in which instructions execute and the data operands involved. See I_{DDIN} calculation in Electrical Characteristics section. Internal power dissipation is calculated this way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

– the number of output pins that switch during each cycle (O)
– the maximum frequency at which the pins can switch (f)
– the load capacitance of the pins (C)
– the voltage swing of the pins (V_{DD}).

The external component is calculated using:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The frequency f includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/t_{CK}$ while in SDRAM burst mode.

Example:

Estimate P_{EXT} with the following assumptions:

– a system with one bank of external memory (32-bit)
– two 1M × 16 SDRAM chips, each with a control signal load of 3 pF and a data signal load of 4 pF
– external data writes occur in burst mode, two every $1/t_{CK}$ cycles, a potential frequency of $1/t_{CK}$ cycles/s. Assume 50% pin switching
– the external SDRAM clock rate is 60 MHz ($2/t_{CK}$).

The P_{EXT} equation is calculated for each class of pins that can drive:

Table V. External Power Calculations

Pin Type	# of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	11	50	× 10.7	× 30 MHz	× 10.9 V	= 0.019 W
$\overline{MS_0}$	1	0	× 10.7	—	× 10.9 V	= 0.000 W
$\overline{SDWE}$	1	0	× 10.7	—	× 10.9 V	= 0.000 W
Data	32	50	× 7.7	× 30 MHz	× 10.9 V	= 0.042 W
SDRAM CLK	1	–	× 10.7	× 30 MHz	× 10.9 V	= 0.007 W

P_{EXT} = 0.068 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation. (I_{DDIN} see calculation in Electrical Characteristics section):

$$P_{TOTAL} = P_{EXT} + (I_{DDIN} \times V_{DD})$$

Note that the conditions causing a worst-case P_{EXT} differ from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones (1s) to all zeros (0s). Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21065L is offered in a 208-lead MQFP and a 196-ball Mini-BGA package.

The ADSP-21065L is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an air flow source may be used.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power Dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation)

θ_{JC} = 7.1°C/W for 208-lead MQFP
θ_{JC} = 5.1°C/W for 196-ball Mini-BGA

Airflow

Table VI. Thermal Characteristics (208-Lead MQFP)

(Linear Ft./Min.)	0	100	200	400	600
θ_{CA} (°C/W)	24	20	19	17	13

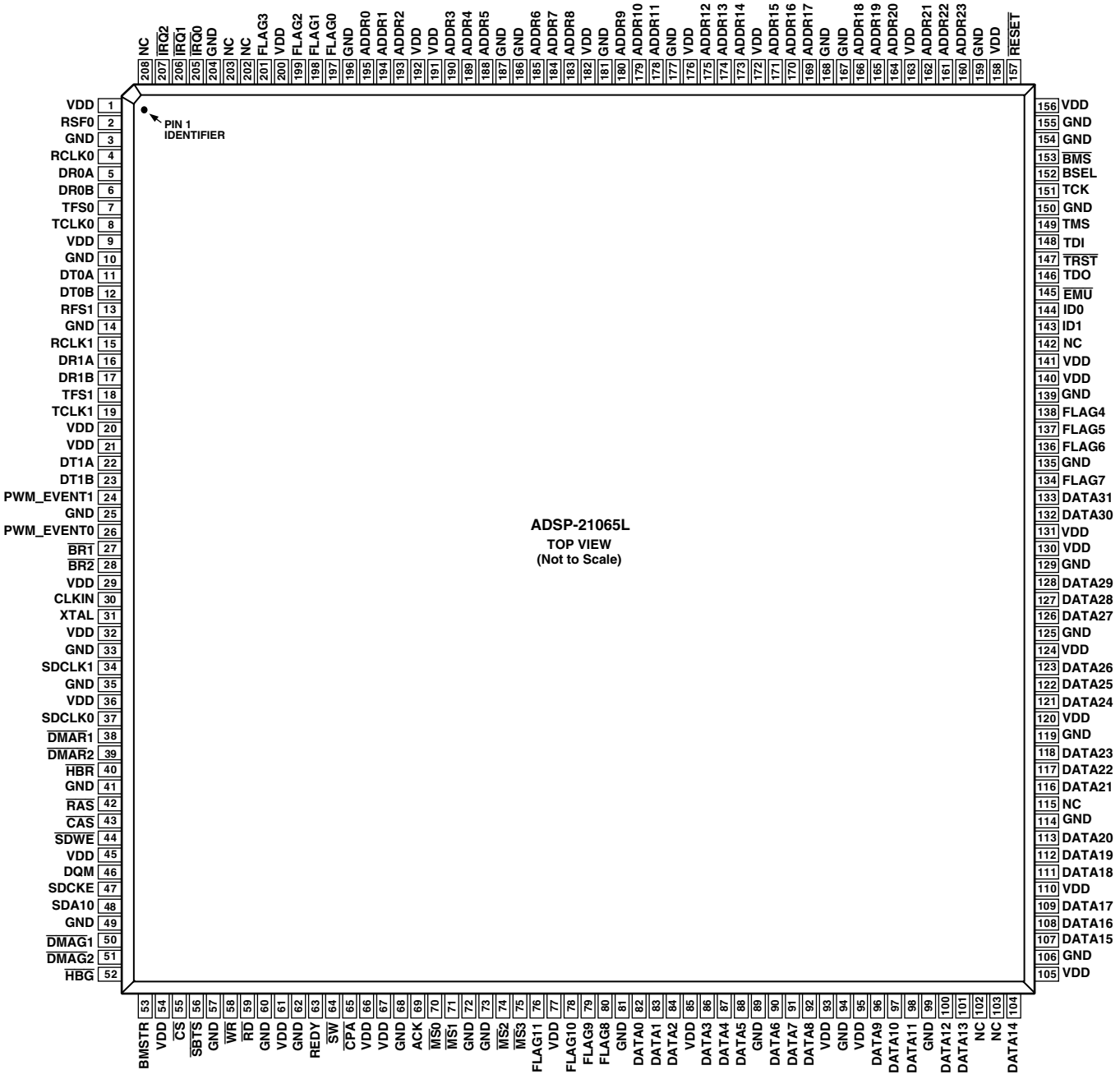
Table VII. 196-Ball Mini-BGA

(Linear Ft./Min.)	0	200	400
θ_{CA} (°C/W)	38	29	23

208-LEAD MQFP PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	43	$\overline{\text{CAS}}$	85	VDD	127	DATA28	169	ADDR17
2	RFS0	44	$\overline{\text{SDWE}}$	86	DATA3	128	DATA29	170	ADDR16
3	GND	45	VDD	87	DATA4	129	GND	171	ADDR15
4	RCLK0	46	DQM	88	DATA5	130	VDD	172	VDD
5	DR0A	47	SDCKE	89	GND	131	VDD	173	ADDR14
6	DR0B	48	SDA10	90	DATA6	132	DATA30	174	ADDR13
7	TFS0	49	GND	91	DATA7	133	DATA31	175	ADDR12
8	TCLK0	50	$\overline{\text{DMAG}}$1	92	DATA8	134	FLAG7	176	VDD
9	VDD	51	$\overline{\text{DMAG}}$2	93	VDD	135	GND	177	GND
10	GND	52	$\overline{\text{HBG}}$	94	GND	136	FLAG6	178	ADDR11
11	DT0A	53	BMSTR	95	VDD	137	FLAG5	179	ADDR10
12	DT0B	54	VDD	96	DATA9	138	FLAG4	180	ADDR9
13	RFS1	55	$\overline{\text{CS}}$	97	DATA10	139	GND	181	GND
14	GND	56	$\overline{\text{SBTS}}$	98	DATA11	140	VDD	182	VDD
15	RCLK1	57	GND	99	GND	141	VDD	183	ADDR8
16	DR1A	58	$\overline{\text{WR}}$	100	DATA12	142	NC	184	ADDR7
17	DR1B	59	$\overline{\text{RD}}$	101	DATA13	143	ID1	185	ADDR6
18	TFS1	60	GND	102	NC	144	ID0	186	GND
19	TCLK1	61	VDD	103	NC	145	$\overline{\text{EMU}}$	187	GND
20	VDD	62	GND	104	DATA14	146	TDO	188	ADDR5
21	VDD	63	REDY	105	VDD	147	$\overline{\text{TRST}}$	189	ADDR4
22	DT1A	64	$\overline{\text{SW}}$	106	GND	148	TDI	190	ADDR3
23	DT1B	65	$\overline{\text{CPA}}$	107	DATA15	149	TMS	191	VDD
24	PWM_EVENT1	66	VDD	108	DATA16	150	GND	192	VDD
25	GND	67	VDD	109	DATA17	151	TCK	193	ADDR2
26	PWM_EVENT0	68	GND	110	VDD	152	BSEL	194	ADDR1
27	$\overline{\text{BR1}}$	69	ACK	111	DATA18	153	$\overline{\text{BMS}}$	195	ADDR0
28	$\overline{\text{BR2}}$	70	$\overline{\text{MS}}$0	112	DATA19	154	GND	196	GND
29	VDD	71	$\overline{\text{MS}}$1	113	DATA20	155	GND	197	FLAG0
30	CLKIN	72	GND	114	GND	156	VDD	198	FLAG1
31	XTAL	73	GND	115	NC	157	$\overline{\text{RESET}}$	199	FLAG2
32	VDD	74	$\overline{\text{MS}}$2	116	DATA21	158	VDD	200	VDD
33	GND	75	$\overline{\text{MS}}$3	117	DATA22	159	GND	201	FLAG3
34	SDCLK1	76	FLAG11	118	DATA23	160	ADDR23	202	NC
35	GND	77	VDD	119	GND	161	ADDR22	203	NC
36	VDD	78	FLAG10	120	VDD	162	ADDR21	204	GND
37	SDCLK0	79	FLAG9	121	DATA24	163	VDD	205	$\overline{\text{IRQ}}$0
38	$\overline{\text{DMAR}}$1	80	FLAG8	122	DATA25	164	ADDR20	206	$\overline{\text{IRQ}}$1
39	$\overline{\text{DMAR}}$2	81	GND	123	DATA26	165	ADDR19	207	$\overline{\text{IRQ}}$2
40	$\overline{\text{HBR}}$	82	DATA0	124	VDD	166	ADDR18	208	NC
41	GND	83	DATA1	125	GND	167	GND		
42	$\overline{\text{RAS}}$	84	DATA2	126	DATA27	168	GND		

208-LEAD MQFP PIN

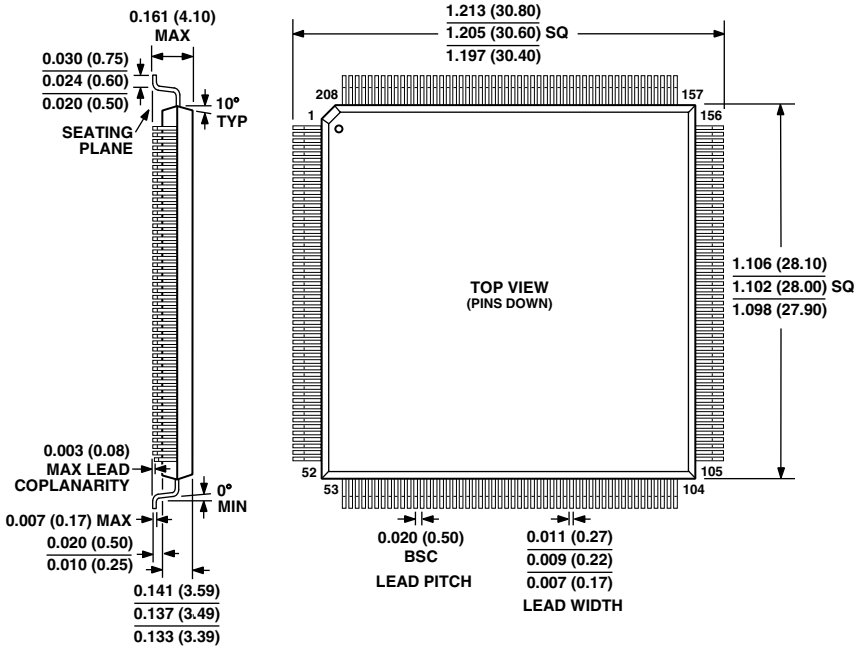


NC = NO CONNECT

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

208-Lead Plastic Quad Flatpack (MQFP)



NOTES

1. THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.003 (0.08) FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.
2. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
3. THE 208 LEAD MQFP IS A METRIC PACKAGE. ENGLISH DIMENSIONS PROVIDED ARE APPROXIMATE AND MUST NOT BE USED FOR BOARD DESIGN PURPOSES.

196-BALL MINI-BGA PIN CONFIGURATION

Ball #	Name	Ball #	Name	Ball #	Name	Ball #	Name	Ball #	Name
A1	NC1	B1	DR0A	C1	TCLK0	D1	RCLK1	E1	TFS1
A2	NC2	B2	RFS0	C2	RCLK0	D2	TFS0	E2	DT0B
A3	FLAG2	B3	IRQ0	C3	IRQ2	D3	DR0B	E3	DT0A
A4	ADDR0	B4	FLAG0	C4	FLAG3	D4	IRQ1	E4	RFS1
A5	ADDR3	B5	ADDR2	C5	ADDR1	D5	FLAG1	E5	VDD
A6	ADDR6	B6	ADDR5	C6	ADDR4	D6	VDD	E6	GND
A7	ADDR7	B7	ADDR9	C7	ADDR10	D7	VDD	E7	GND
A8	ADDR8	B8	ADDR12	C8	ADDR13	D8	VDD	E8	GND
A9	ADDR11	B9	ADDR15	C9	ADDR16	D9	VDD	E9	GND
A10	ADDR14	B10	ADDR19	C10	ADDR20	D10	VDD	E10	VDD
A11	ADDR17	B11	ADDR21	C11	ADDR22	D11	BMS	E11	ID0
A12	ADDR18	B12	ADDR23	C12	RESET	D12	TMS	E12	TDI
A13	NC8	B13	GND	C13	BSEL	D13	TRST	E13	ID1
A14	NC7	B14	TCK	C14	TDO	D14	EMU	E14	FLAG4
F1	TCLK1	G1	PWM_ EVENT1	H1	PWM_ EVENT0	J1	CLKIN	K1	DMAR1
F2	DR1B	G2	DT1B	H2	BR1	J2	XTAL	K2	SDCLK0
F3	DR1A	G3	DT1A	H3	BR2	J3	SDCLK1	K3	HBR
F4	VDD	G4	VDD	H4	VDD	J4	VDD	K4	SDWE
F5	GND	G5	GND	H5	GND	J5	GND	K5	VDD
F6	GND	G6	GND	H6	GND	J6	GND	K6	GND
F7	GND	G7	GND	H7	GND	J7	GND	K7	GND
F8	GND	G8	GND	H8	GND	J8	GND	K8	GND
F9	GND	G9	GND	H9	GND	J9	GND	K9	GND
F10	GND	G10	GND	H10	GND	J10	GND	K10	VDD
F11	VDD	G11	VDD	H11	VDD	J11	VDD	K11	DATA19
F12	FLAG6	G12	DATA31	H12	DATA28	J12	DATA24	K12	DATA21
F13	FLAG5	G13	DATA30	H13	DATA27	J13	DATA25	K13	DATA20
F14	FLAG7	G14	DATA29	H14	DATA26	J14	DATA23	K14	DATA22
L1	DMAR2	M1	RAS	N1	DQM	P1	NC3		
L2	CAS	M2	SDCKE	N2	HBG	P2	NC4		
L3	SDA10	M3	DMAG1	N3	BMSTR	P3	GND		
L4	DMAG2	M4	CS	N4	SBTS	P4	WR		
L5	VDD	M5	RD	N5	REDY	P5	SW		
L6	VDD	M6	CPA	N6	GND	P6	MS0		
L7	VDD	M7	ACK	N7	MS1	P7	MS2		
L8	VDD	M8	FLAG10	N8	FLAG11	P8	MS3		
L9	VDD	M9	DATA2	N9	DATA1	P9	FLAG9		
L10	DATA8	M10	DATA5	N10	DATA4	P10	FLAG8		
L11	DATA13	M11	DATA9	N11	DATA7	P11	DATA0		
L12	DATA16	M12	DATA12	N12	DATA10	P12	DATA3		
L13	DATA17	M13	DATA14	N13	DATA11	P13	DATA6		
L14	DATA18	M14	DATA15	N14	NC6	P14	NC5		

196-BALL MINI-BGA PIN CONFIGURATION

14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC7	NC8	ADDR18	ADDR17	ADDR14	ADDR11	ADDR8	ADDR7	ADDR6	ADDR3	ADDR0	FLAG2	NC2	NC1	A
TCK	GND	ADDR23	ADDR21	ADDR19	ADDR15	ADDR12	ADDR9	ADDR5	ADDR2	FLAG0	$\overline{\text{IRQ0}}$	RFS0	DR0A	B
TDO	BSEL	$\overline{\text{RESET}}$	ADDR22	ADDR20	ADDR16	ADDR13	ADDR10	ADDR4	ADDR1	FLAG3	$\overline{\text{IRQ2}}$	RCLK0	TCLK0	C
$\overline{\text{EMU}}$	$\overline{\text{TRST}}$	TMS	$\overline{\text{BMS}}$	VDD	VDD	VDD	VDD	VDD	FLAG1	$\overline{\text{IRQ1}}$	DR0B	TFS0	RCLK1	D
FLAG4	ID1	TDI	ID0	VDD	GND	GND	GND	GND	VDD	RFS1	DT0A	DT0B	TFS1	E
FLAG7	FLAG5	FLAG6	VDD	GND	GND	GND	GND	GND	GND	VDD	DR1A	DR1B	TCLK1	F
DATA29	DATA30	DATA31	VDD	GND	GND	GND	GND	GND	GND	VDD	DT1A	DT1B	PWM_ EVENT1	G
DATA26	DATA27	DATA28	VDD	GND	GND	GND	GND	GND	GND	VDD	$\overline{\text{BR2}}$	$\overline{\text{BR1}}$	PWM_ EVENT0	H
DATA23	DATA25	DATA24	VDD	GND	GND	GND	GND	GND	GND	VDD	SDCLK1	XTAL	CLKIN	J
DATA22	DATA20	DATA21	DATA19	VDD	GND	GND	GND	GND	VDD	$\overline{\text{SDWE}}$	$\overline{\text{HBR}}$	SDCLK0	$\overline{\text{DMAR1}}$	K
DATA18	DATA17	DATA16	DATA13	DATA8	VDD	VDD	VDD	VDD	VDD	$\overline{\text{DMAG2}}$	SDA10	$\overline{\text{CAS}}$	$\overline{\text{DMAR2}}$	L
DATA15	DATA14	DATA12	DATA9	DATA5	DATA2	FLAG10	ACK	$\overline{\text{CPA}}$	$\overline{\text{RD}}$	$\overline{\text{CS}}$	$\overline{\text{DMAG1}}$	SDCKE	$\overline{\text{RAS}}$	M
NC6	DATA11	DATA10	DATA7	DATA4	DATA1	FLAG11	$\overline{\text{MS1}}$	GND	REDY	$\overline{\text{SBTS}}$	BMSTR	$\overline{\text{HBG}}$	DQM	N
NC5	DATA6	DATA3	DATA0	FLAG8	FLAG9	$\overline{\text{MS3}}$	$\overline{\text{MS2}}$	$\overline{\text{MS0}}$	$\overline{\text{SW}}$	$\overline{\text{WR}}$	GND	NC4	NC3	P

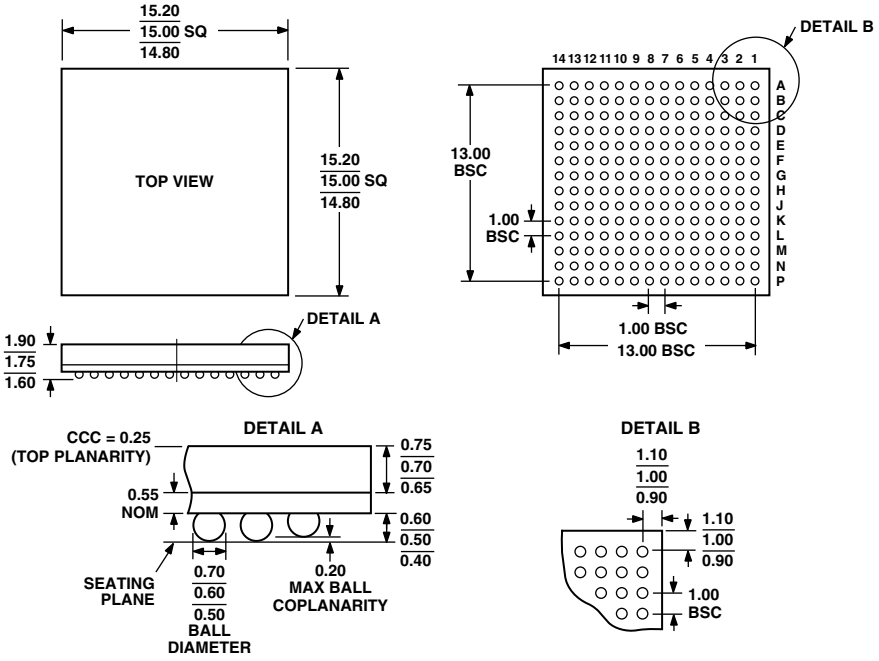
ORDERING GUIDE

Part Number	Case Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Options
ADSP-21065LKS-240	0°C to +85°C	60 MHz	544 Kbit	3.3 V	MQFP
ADSP-21065LCS-240	–40°C to +100°C	60 MHz	544 Kbit	3.3 V	MQFP
ADSP-21065LKCA-240	0°C to +85°C	60 MHz	544 Kbit	3.3 V	Mini-BGA
ADSP-21065LKS-264	0°C to +85°C	66 MHz	544 Kbit	3.3 V	MQFP
ADSP-21065LKCA-264	0°C to +85°C	66 MHz	544 Kbit	3.3 V	Mini-BGA

OUTLINE DIMENSIONS

Dimensions shown in mm.

196-Ball Mini-BGA



NOTES

1. THE ACTUAL POSITION OF THE BALL GRID IS WITHIN 0.30 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.10 OF ITS IDEAL POSITION RELATIVE TO THE BALL GRID.
2. ALL MEASUREMENTS ARE PROVIDED IN METRIC UNITS BECAUSE THIS IS A METRIC PACKAGE. ANALOG DEVICES STRONGLY RECOMMENDS THAT YOU DESIGN WITH THE METRIC MEASUREMENTS ONLY.
3. BALL DIAMETER HAS BEEN CHANGED FROM 0.50mm NOMINAL TO 0.60mm NOMINAL TO COMPLY WITH JEDEC STANDARD PUBLICATION 95 CASE OUTLINE DRAWING MO–151. 0.60 NOMINAL BALL DIAMETER PRODUCT WILL BE AVAILABLE IN JULY, 2000.

C3533b–3–5/00 (rev. B) 00172

PRINTED IN U.S.A.