

DATA SHEET

74AHC1G08; 74AHCT1G08 2-input AND gate

Product specification
Supersedes data of 1998 Nov 25
File under Integrated Circuits, IC06

1999 Jan 27

2-input AND gate

74AHC1G08; 74AHCT1G08

FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V
- Low power dissipation
- Balanced propagation delays
- Very small 5-pin package
- Output capability: standard.

DESCRIPTION

The 74AHC1G/AHCT1G08 is a high-speed Si-gate CMOS device.

The 74AHC1G/AHCT1G08 provides the 2-input AND function.

FUNCTION TABLE

See note 1.

| INPUTS | | OUTPUT |
|--------|-----|--------|
| inA | inB | outY |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

Note

1. H = HIGH voltage level.
L = LOW voltage level.

ORDERING AND PACKAGE INFORMATION

| TYPE NUMBER | PACKAGES | | | | | |
|--------------|-------------------|------|---------|----------|--------|---------|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE | MARKING |
| 74AHC1G08GW | -40 to +85 °C | 5 | SC-88A | plastic | SOT353 | AE |
| 74AHCT1G08GW | | 5 | SC-88A | plastic | SOT353 | CE |

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ °C}$; $t_r = t_f \leq 3.0\text{ ns}$.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|------------------------------------|--|---------|--------|------|
| | | | AHC1G | AHCT1G | |
| t_{PHL}/t_{PLH} | propagation delay inA, inB to outY | $C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$ | 3.2 | 3.6 | ns |
| C_I | input capacitance | | 1.5 | 1.5 | pF |
| C_{PD} | power dissipation capacitance | notes 1 and 2; $C_L = 50\text{ pF}$; $f = 1\text{ MHz}$ | 17 | 19 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V.
2. The condition is $V_I = \text{GND}$ to V_{CC} .

PINNING

| PIN | SYMBOL | DESCRIPTION |
|-----|----------|-------------------|
| 1 | inB | data input |
| 2 | inA | data input |
| 3 | GND | ground (0 V) |
| 4 | outY | data output |
| 5 | V_{CC} | DC supply voltage |

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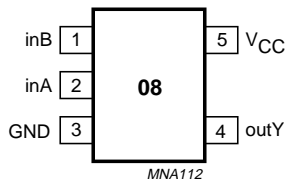


Fig.1 Pin configuration.

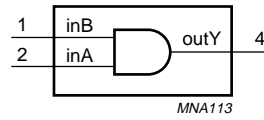


Fig.2 Logic symbol.

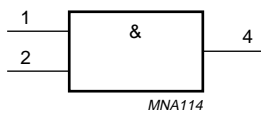


Fig.3 IEC logic symbol.

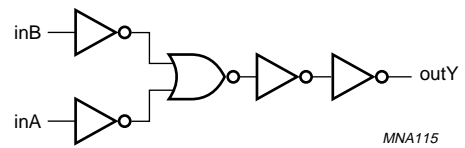


Fig.4 Logic diagram.

2-input AND gate

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | 74AHC1G | | | 74AHCT1G | | | UNIT |
|--------------------------------|---|--|---------|------|----------|----------|------|----------|------|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| V_{CC} | DC supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | – | 5.5 | 0 | – | 5.5 | V |
| V_O | output voltage | | 0 | – | V_{CC} | 0 | – | V_{CC} | V |
| T_{amb} | operating ambient temperature range | see DC and AC characteristics per device | –40 | +25 | +85 | –40 | +25 | +85 | °C |
| $t_r, t_f (\Delta t/\Delta f)$ | input rise and fall times except for Schmitt-trigger inputs | $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5 V \pm 0.5 V$ | – | – | 100 | – | – | – | ns/V |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|----------------------------------|---|------|------|------|
| V_{CC} | DC supply voltage | | –0.5 | +7.0 | V |
| V_I | input voltage range | | –0.5 | +7.0 | V |
| I_{IK} | DC input diode current | $V_I < -0.5$ | – | –20 | mA |
| I_{OK} | DC output diode current | $V_O < -0.5$ or $V_O > V_{CC} + 0.5 V$; note 1 | – | ±20 | mA |
| I_O | DC output source or sink current | $-0.5 V < V_O < V_{CC} + 0.5 V$ | – | ±25 | mA |
| I_{CC} | DC V_{CC} or GND current | | – | ±75 | mA |
| T_{stg} | storage temperature range | | –65 | +150 | °C |
| P_D | power dissipation per package | temperature range: –40 to +85 °C; note 2 | – | 200 | mW |

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- Above +55 °C the value of P_D derates linearly with 2.5 mW/K.

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DC CHARACTERISTICS

Family 74AHC1G

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | T _{amb} (°C) | | | | | UNIT |
|-----------------|--|---|---------------------|-----------------------|------|------|------------|------|------|
| | | OTHER | V _{CC} (V) | +25 | | | -40 to +85 | | |
| | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| V _{IH} | HIGH-level input voltage | | 2.0 | 1.5 | – | – | 1.5 | – | V |
| | | | 3.0 | 2.1 | – | – | 2.1 | – | |
| | | | 5.5 | 3.85 | – | – | 3.85 | – | |
| V _{IL} | LOW-level input voltage | | 2.0 | – | – | 0.5 | – | 0.5 | V |
| | | | 3.0 | – | – | 0.9 | – | 0.9 | |
| | | | 5.5 | – | – | 1.65 | – | 1.65 | |
| V _{OH} | HIGH-level output voltage; all outputs | V _I = V _{IH} or V _{IL} ; I _O = –50 μA | 2.0 | 1.9 | 2.0 | – | 1.9 | – | V |
| | | | 3.0 | 2.9 | 3.0 | – | 2.9 | – | |
| | | | 4.5 | 4.4 | 4.5 | – | 4.4 | – | |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; I _O = –4.0 mA | 3.0 | 2.58 | – | – | 2.48 | – | V |
| | | V _I = V _{IH} or V _{IL} ; I _O = –8.0 mA | 4.5 | 3.94 | – | – | 3.8 | – | |
| V _{OL} | LOW-level output voltage; all outputs | V _I = V _{IH} or V _{IL} ; I _O = 50 μA | 2.0 | – | 0 | 0.1 | – | 0.1 | V |
| | | | 3.0 | – | 0 | 0.1 | – | 0.1 | |
| | | | 4.5 | – | 0 | 0.1 | – | 0.1 | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; I _O = 4 mA | 3.0 | – | – | 0.36 | – | 0.44 | V |
| | | V _I = V _{IH} or V _{IL} ; I _O = 8 mA | 4.5 | – | – | 0.36 | – | 0.44 | |
| I _I | input leakage current | V _I = V _{CC} or GND | 5.5 | – | – | 0.1 | – | 1.0 | μA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 | 5.5 | – | – | 1.0 | – | 10 | μA |
| C _I | input capacitance | | | – | 1.5 | 10 | – | 10 | pF |

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Family 74AHCT1G

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | T _{amb} (°C) | | | | | UNIT |
|------------------|---|--|---------------------|-----------------------|------|------|------------|------|------|
| | | OTHER | V _{CC} (V) | +25 | | | -40 to +85 | | |
| | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| V _{IH} | HIGH-level input voltage | | 4.5 to 5.5 | 2.0 | – | – | 2.0 | – | V |
| V _{IL} | LOW-level input voltage | | 4.5 to 5.5 | – | – | 0.8 | – | 0.8 | V |
| V _{OH} | HIGH-level output voltage; all outputs | V _I = V _{IH} or V _{IL} ; I _O = –50 µA | 4.5 | 4.4 | 4.5 | – | 4.4 | – | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; I _O = –8.0 mA | 4.5 | 3.94 | – | – | 3.8 | – | V |
| V _{OL} | LOW-level output voltage; all outputs | V _I = V _{IH} or V _{IL} ; I _O = 50 µA | 4.5 | – | 0 | 0.1 | – | 0.1 | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; I _O = 8 mA | 4.5 | – | – | 0.36 | – | 0.44 | V |
| I _I | input leakage current | V _I = V _{IH} or V _{IL} | 5.5 | – | – | 0.1 | – | 1.0 | µA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 | 5.5 | – | – | 1.0 | – | 10 | µA |
| ΔI _{CC} | additional quiescent supply current per input pin | V _I = 3.4 V other inputs at V _{CC} or GND; I _O = 0 | 5.5 | – | – | 1.35 | – | 1.5 | mA |
| C _I | input capacitance | | | – | 1.5 | 10 | – | 10 | pF |

2-input AND gate

74AHC1G08; 74AHCT1G08

AC CHARACTERISTICS

Type 74AHC1G08

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

| SYMBOL | PARAMETER | TEST CONDITIONS | | | T _{amb} (°C) | | | | | UNIT |
|------------------------------------|---------------------------------------|------------------|----------------|---------------------|-----------------------|--------------------|------|------------|------|------|
| | | WAVEFORMS | C _L | V _{CC} (V) | +25 | | | -40 to +85 | | |
| | | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| t _{PHL} /t _{PLH} | propagation delay inA, inB to outY | see Figs 5 and 6 | 15 pF | 3.0 to 3.6 | – | 4.6 ⁽¹⁾ | 8.8 | 1.0 | 10.5 | ns |
| t _{PHL} /t _{PLH} | propagation delay inA, inB to outY | see Figs 5 and 6 | 50 pF | 3.0 to 3.6 | – | 6.5 ⁽¹⁾ | 12.3 | 1.0 | 14.0 | ns |
| t _{PHL} /t _{PLH} | propagation delay inA, inB to outY | see Figs 5 and 6 | 15 pF | 4.5 to 5.5 | – | 3.2 ⁽²⁾ | 5.9 | 1.0 | 7.0 | ns |
| t _{PHL} /t _{PLH} | propagation delay inA, inB to outY | see Figs 5 and 6 | 50 pF | 4.5 to 5.5 | – | 4.6 ⁽²⁾ | 7.9 | 1.0 | 9.0 | ns |

Notes

1. Typical values at V_{CC} = 3.3 V.
2. Typical values at V_{CC} = 5.0 V.

Type 74AHCT1G08

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

| SYMBOL | PARAMETER | TEST CONDITIONS | | | T _{amb} (°C) | | | | | UNIT |
|------------------------------------|---------------------------------------|------------------|----------------|---------------------|-----------------------|--------------------|------|------------|------|------|
| | | WAVEFORMS | C _L | V _{CC} (V) | +25 | | | -40 to +85 | | |
| | | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| t _{PHL} /t _{PLH} | propagation delay inA, inB to outY | see Figs 5 and 6 | 15 pF | 4.5 to 5.5 | – | 3.6 ⁽¹⁾ | 6.9 | 1.0 | 8.0 | ns |
| t _{PHL} /t _{PLH} | propagation delay inA, inB to outY | see Figs 5 and 6 | 50 pF | 4.5 to 5.5 | – | 5.1 ⁽¹⁾ | 7.9 | 1.0 | 9.0 | ns |

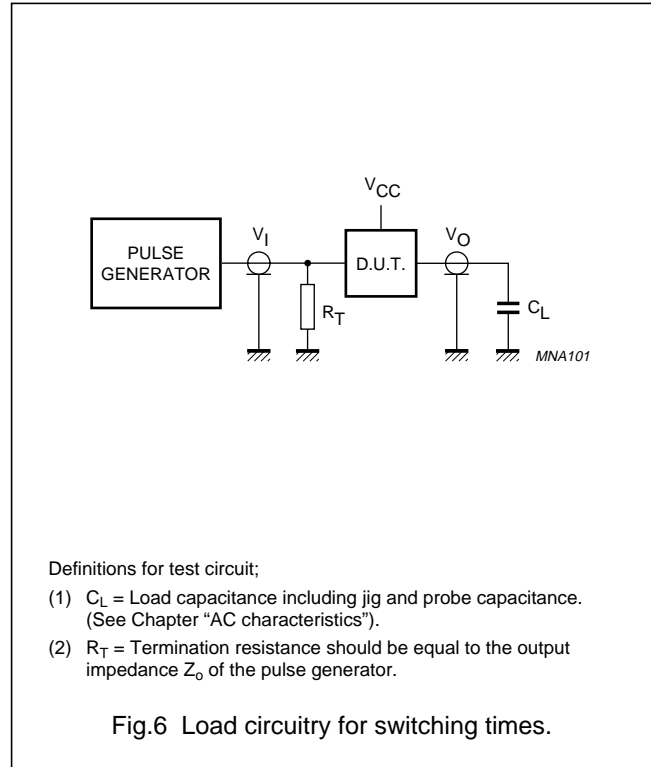
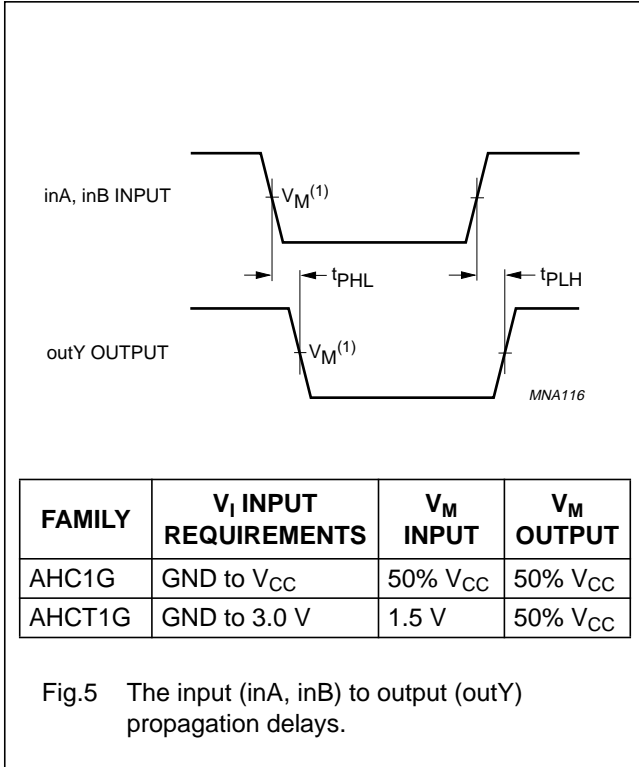
Note

1. Typical values at V_{CC} = 5.0 V.

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AC WAVEFORMS



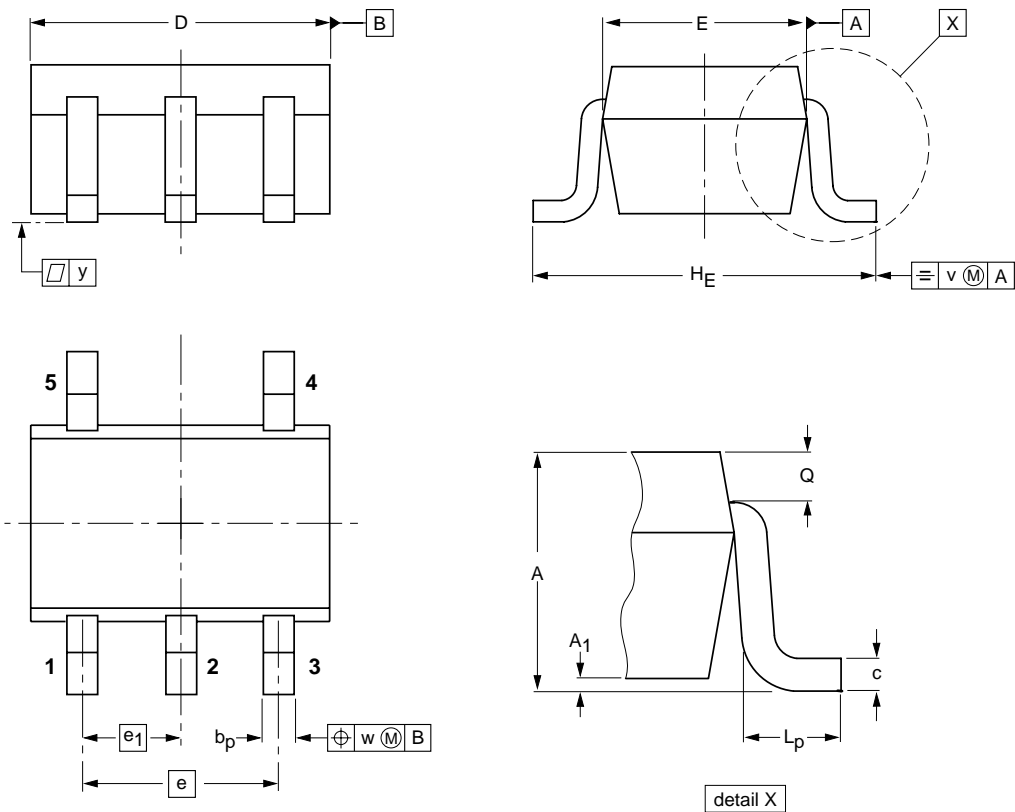
2-input AND gate

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PACKAGE OUTLINE

Plastic surface mounted package; 5 leads

SOT353



DIMENSIONS (mm are the original dimensions)

| UNIT | A | A ₁ max | b _p | c | D | E ⁽²⁾ | e | e ₁ | H _E | L _p | Q | v | w | y |
|------|------------|-----------------------|----------------|--------------|------------|------------------|-----|----------------|----------------|----------------|--------------|-----|-----|-----|
| mm | 1.1 0.8 | 0.1 | 0.30 0.20 | 0.25 0.10 | 2.2 1.8 | 1.35 1.15 | 1.3 | 0.65 | 2.2 2.0 | 0.45 0.15 | 0.25 0.15 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|--------|--|------------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT353 | | | SC-88A | | | 97-02-28 |

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|-------------------------------|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 489 4339/4239, Fax. +30 1 481 4240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
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Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
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Uruguay: see South America

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