

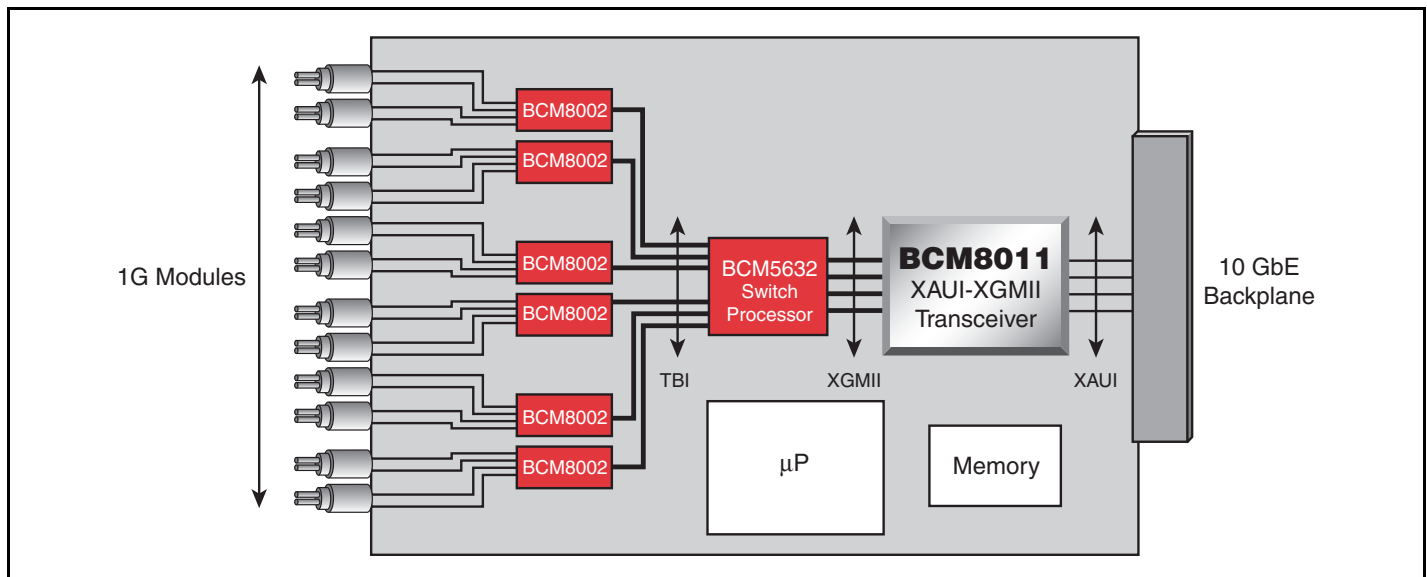
FOUR-CHANNEL 3.125 GIGABIT ETHERNET CMOS TRANSCEIVER

FEATURES

- Support for four channels of 3.125 GigaBaud per second (GBd) resulting in an effective aggregate data rate of 10 Gigabits per second (Gbps)
- Support for the 10 Gigabit attachment unit (XAUI) and 10 Gigabit media independent interface (XGMII) proposed by the IEEE 802.3ae standards
- Less than 3 ps Root Mean Square (RMS) transmit jitter using Broadcom's LC-VCO technology
- 32 bytes of de-skewing capability for the channels
- 32-bit parallel interface compatible to SSTL_2/HSTL (1.5) Class I EIA/JEDEC specifications
- On-chip phase-locked loop (PLL), providing clock synthesis from 156.25 MHz clock references
- Optional 8B/10B encoder and 10B/8B decoder in each channel
- Parallel or serial loopback modes
- Built-In Self-Test (BIST) capability
- Termination resistors on-chip
- Implemented in a 0.18μ standard CMOS process technology (1.8V and 2.5V supplies)
- 2.5W nominal power
- 324-pin FBGA package (19 mm x 19 mm)

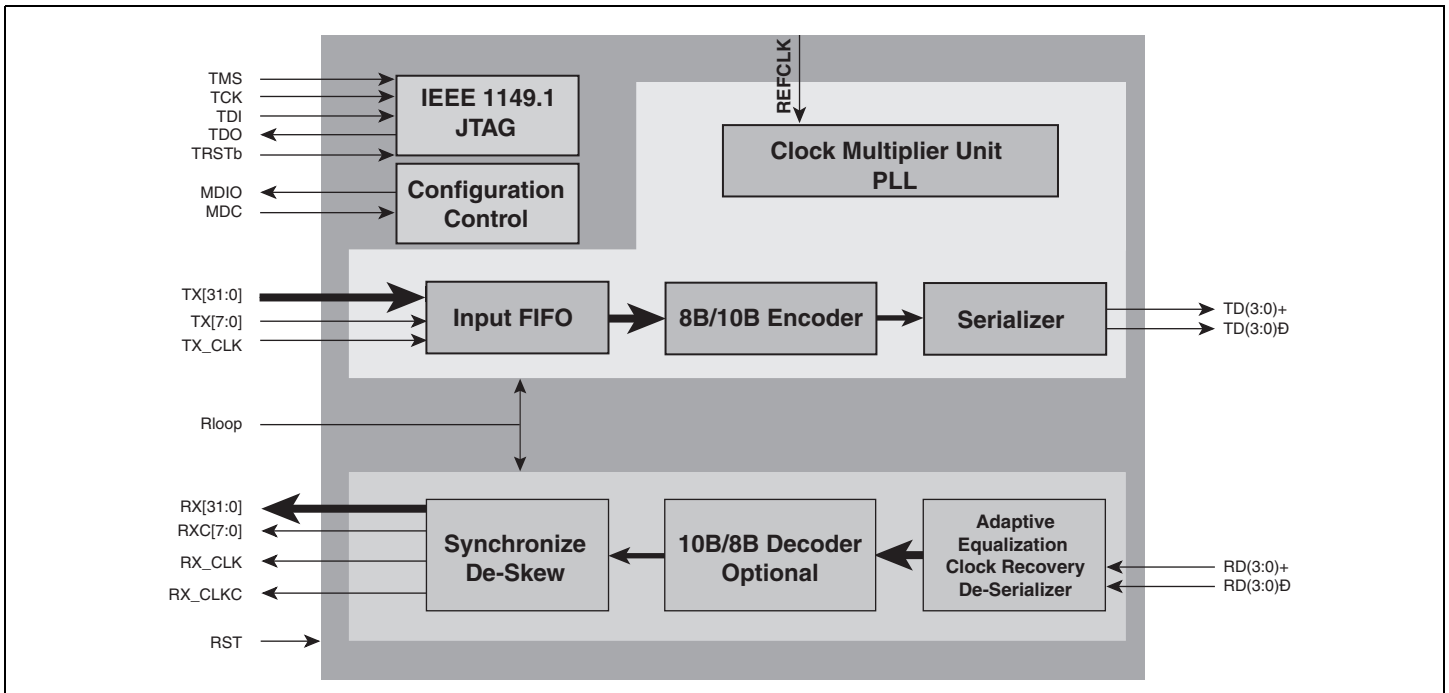
SUMMARY OF BENEFITS

- Enables data transfer rate of 10 Gbps over metropolitan network when used with wavelength division multiplexing (WDM) or XAUI interface to a serial 10-Gbps laser module.
- Ultra-low transmitter jitter on each channel results in a longer cable reach (in excess of 40 km).
- EyeOpener™ adaptive equalizer extends the speed and reach of copper traces over FR4 backplane.
- Adaptive equalization and ultra-low receiver jitter enhance the receive eye pattern, which results in a superb bit-error rate (BER).
- Easy-to-use programming of the global configuration registers facilitates the design of the system. It provides enable/disable functions such as PLL lock, channel synchronization, VCO bypass, serial and loopback modes for self-diagnosis, and selecting source-centered and source-synchronous clocking.
- In-system at-speed link and on-board Built-In-Self-Test (BIST) is available using programmable pseudo-random bit sequence (PRBS) and programmable pattern comparators.



Application Diagram

OVERVIEW



The BCM8011 chip provides an aggregate bandwidth of 10-Gbps full-duplex, extending Ethernet capabilities into the Wide Area Network (WAN). The BCM8011 integrates four channels of the Broadcom FusionCore™ - a high-performance mixed-signal transceiver core, capable of transmitting and receiving data at 3.125 Gigabits per second (Gbps).

The chip also supports Broadcom's EyeOpener™ adaptive equalizer, which improves overall cable reach and compensates for the electrical imperfections associated with the copper traces and connectors.

Fully integrated PLL and Clock and Data Recovery enable individual channels to lock to the incoming data. The unique design of the LC-VCO and CDR blocks have resulted in a less than 3 ps Root Mean Square (RMS) transmit jitter implemented in CMOS.

The transmitter section accepts 32-bit-wide (XGMII) parallel SSTL_2/HSTL-compatible data, clock and control signals and serializes the 32-bit data into a 4-differential pair of CML high-speed data (XAUI).

The receiver section enables individual channels to lock to the incoming data. The recovered data is presented at the SSTL_2/HSTL-compatible parallel outputs.

The optional 8B/10B encoding and 10B/8B decoding of the PCS layer are integrated in the transceiver. Channel alignment and synchronization capabilities are addressed through configuration registers.

Broadcom also offers a complete evaluation kit, including board and related software running on the Microsoft® Windows® 98 or Windows® NT 4.0.

Applications:

- 10 Gigabit Ethernet LAN, MAN, WAN switches and routers
- Next-generation network interface cards
- Fiber headends
- Advanced Test Equipment (ATE)
- High-speed serial copper connections

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BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

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Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com