**Synchronous DRAM** **512K x 16 Bit x 2 Banks**

## General Description

The ADS4616A4A are two-bank Synchronous DRAMs organized as 524,288 words x 16 bits x 2 banks,

Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle.

Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth high performance memory system applications

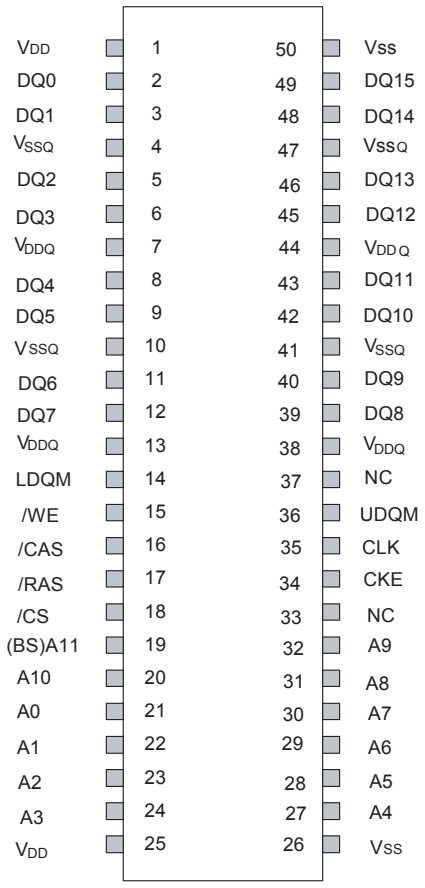
## Features

- Single 3.3V +/- 0.3V power supply
- MRS Cycle with address key programs
  - -CAS Latency (2 & 3)
  - -Burst Length (1,2,4,8, & full page)
  - -Burst Type (sequential & Interleave)
- 2 banks operation
- All inputs are sampled at the positive edge of the system clock
- Burst Read single write operation
- Auto & Self refresh
- 4096 refresh cycle
- DQM for masking
- Package:50-pins 400 mil TSOP-Type II

## Ordering Information.

| Part No. | Frequency | Interface | Package |
|---|---|---|---|
| ADS4616A4A-5 | 200Mhz | LVTTL | 400mil 50pin TSOPII |
| ADS4616A4A -6 | 166Mhz | LVTTL | 400mil 50pin TSOPII |
| ADS4616A4A -7 | 143Mhz | LVTTL | 400mil 50pin TSOPII |

## Pin Assignment

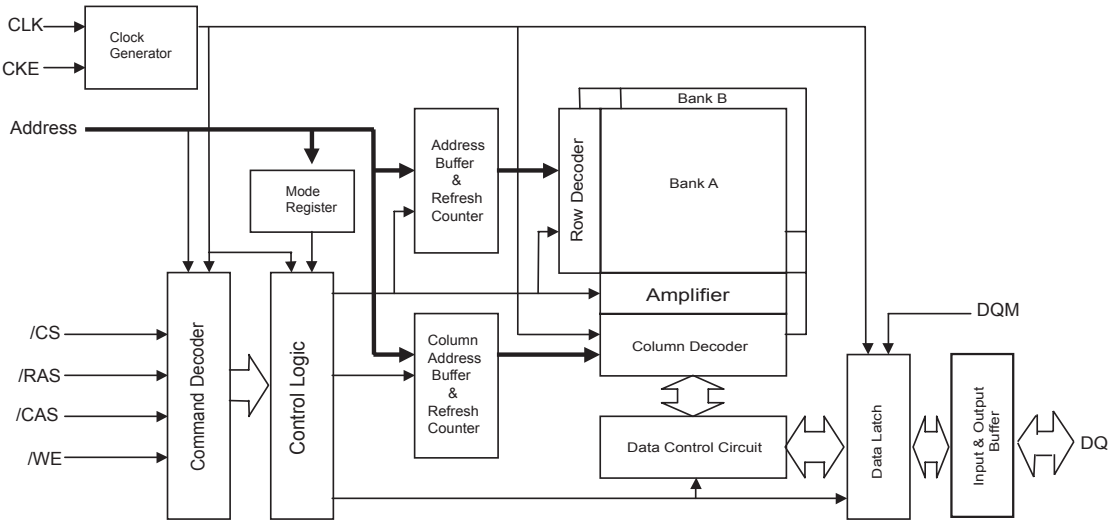



50-pin plastic TSOP II 400 mil

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| CLK | System Clock | Active on the positive edge to sample all inputs. |
| CKE | Clock Enable | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby |
| /CS | Chip Select | Disables or Enables device operation by masking or enabling all input except CLK, CKE and L(U)DQM |
| A0~A10 | Address | Row / Column address are multiplexed on the same pins.<br>Row address : A0~A10<br>Column address : A0~A7 |
| DQ0~DQ15 | Data | Data inputs / outputs are multiplexed on the same pins. |
| L(U)DQM | Data Mask | Makes data output Hi-Z, |
| /RAS | Row Address Strobe | Latches row addresses on the positive edge of the CLK with /RAS low |
| /CAS | Column Address Strobe | Latches Column addresses on the positive edge of the CLK with /CAS low |
| /WE | Write Enable | Enables write operation and row recharge. |
| VDD/VSS | Power Supply/Ground | Power and Ground for the input buffers and the core logic. |
| $V_{DDQ}$/$V_{SSQ}$ | Data Output Power/Ground | Power supply for output buffers. |
| NC | No Connection | This pin is recommended to be left No Connection on the device. |

## Block Diagram



## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$, $V_{out}$ | -0.3~ 4.6 | V |
| Voltage on VDD supply relative to Vss | $V_{DD}$, $V_{DDQ}$ | -0.3~ 4.6 | V |
| Storage temperature | $T_{STG}$ | -55 ~ +150 | ℃ |
| Power dissipation | $P_D$ | 1 | W |
| Short circuit current | $I_{OS}$ | 50 | mA |

**Note :** Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC Operating Condition

Voltage referenced to Vss = 0V, $T_A$ = 0 to 70 ℃

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$, $V_{DDQ}$ | 3.0 | 3.3 | 3.6 | V | |
| Input logic high voltage | $V_{IH}$ | 2.0 | | $V_{DD}$+0.3 | V | 1 |
| Input logic low voltage | $V_{IL}$ | -0.3 | | 0.8 | V | 2 |
| Output logic high voltage | $V_{OH}$ | 2.4 | - | - | V | $I_{OH}$=-2mA |
| Output logic low voltage | $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$=2mA |
| Input leakage current | $I_{IL}$ | -5 | - | 5 | uA | 3 |
| Output leakage current | $I_{OL}$ | -5 | - | 5 | uA | 4 |

**Note :** 1. $V_{IH}$ (max)=$V_{DDH}$+2.0V with a pulse width < 3ns

2.$V_{IL}$(min)=$V_{SSQ}$-2.0V with a pulse < 3ns and – 1.5V with a pulse < 5ns

3.Any input 0V ≦ $V_{IN}$ ≦ $V_{DD}$ + 0.3V, all other pins are not under test = 0V.

4.Dout is disabled, 0V ≦ $V_{OUT}$ ≦ $V_{DD}$.

## AC Operating Condition

Voltage referenced to Vss = 0V, $T_A$ = 0 to 70 ℃

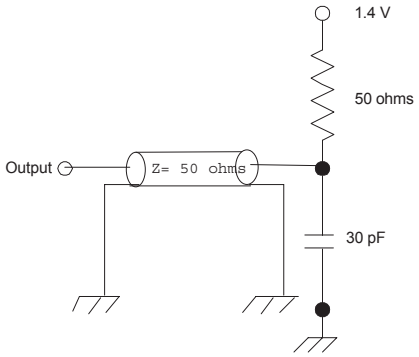
| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| AC input high / low level voltage | $V_{IH}$ / $V_{IL}$ | 1.4 / 1.4 | V | |
| Input timing measurement reference level voltage | Vtrip | 1.4 | V | |
| Input rise / fall time | TR / tF | 1 | ns | |
| Output timing measurement reference level | Voutfef | 1.4 | V | |
| Output load capacitance for access time measurement | CL | 50 | pF | |

## Capacitance

TA=25℃, f-=1Mhz, VDD=3.3V

| Parameter | Pin | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | CLK | C11 | 2.5 | 4 | pF |
| | A0~A11,BA0,BA1,CKE,/CS,/RAS, /CAS,/WE,DQM | C12 | 2.5 | 5 | pF |
| Data input / output capacitance | DQM | CI/O | 4 | 6.5 | pF |

## Output load circuit




## DC Characteristics I

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | -5 | 5 | uA | 1 |
| Output leakage current | $I_{LO}$ | -5 | 5 | uA | 2 |
| Output high voltage | $V_{OH}$ | 2.4 | - | V | $I_{OH}$ = -2mA |
| Output low voltage | $V_{OL}$ | - | 0.4 | V | $I_{OL}$ = 2mA |

**Note :** 1.$V_{IN}$ = 0 TO 3.6V, All other pins are not tested under $V_{IN}$ = 0V.

2.$D_{OUT}$ is disabled, $V_{OUT}$ = 0 to 3.6.

## DC Characteristics II

| Parameter | Symbol | Test condition | Speed | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | -5 | -6 | -7 | | |
| Operating Current | IDD1 | Burst length=1, One bank active tRC≧tRC(min),IOL=0mA | 70 | 60 | 50 | mA | 1 |
| Precharge standby current in power down mode | IDD2P | CKE≦VIL(max), tCK=min | 1 | | | mA | |
| | IDD2PS | CKE≦VIL(max), tCK=∞ | 1 | | | | |
| Precharge standby current in Non power down mode | IDD2N | CKE≧VIH(min), /CS≧VIH(min), tCK=min input signals are changed one time during 2clks. All other pins ≧VDD-0.2V or ≦ 0.2V | 35 | 30 | 25 | mA | |
| | IDD2NS | CKE≧VIH(min), tCK=∞ Input signals are stable. | 8 | | | | |
| Active standby current in power down mode | IDD3P | CKE≦VIL(max), tCK=min | 45 | 40 | 35 | mA | |
| Active standby current in Non power down mode | IDD3N | CKE≧VIH(min), /CS≧VIH(min), tCK=min input signals are changed one time during 2clks. All other pins ≧VDD-0.2V or ≦ 0.2V | 3 | | | mA | |
| Burst mode operating current | IDD4 | tCK≧tCK(min),IOL=0 mA All banks active | 120 | 110 | 100 | mA | 1 |
| Auto refresh current | IDD5 | tRRC≧tRRC(min), All banks active | 60 | 55 | 50 | mA | 2 |
| Self refresh current | IDD6 | CKE≦0.2V | 200 | | | uA | |

**Note:** 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.

2. Min. of tRRC is shown at AC characteristics.

## AC Characteristics

| Parameter | | Symbol | -5 | | -6 | | -7 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| System clock Cycle time | /CAS Latency = 3 | tCK3 | 5 | 1000 | 6 | 1000 | 7 | 1000 | ns | |
| | /CAS Latency = 2 | tCK2 | 7 | | 8 | | 10 | | | |
| Clock high pulse width | | tCHW | 2 | - | 2 | - | 2 | - | ns | 1 |
| Clock low pulse width | | tCLW | 2 | - | 2 | - | 2 | - | ns | 1 |
| Access time form clock | /CAS Latency = 3 | tAC3 | - | 4.5 | - | 5 | - | 5 | ns | 2 |
| | /CAS Latency = 2 | tAC2 | - | 4.5 | - | 5.5 | - | 5.5 | | |
| Row cycle time | | tRC | 54 | - | 60 | - | 65 | - | ns | |
| /RAS to /CAS delay | | tRCD | 14 | - | 18 | - | 20 | - | ns | |
| /RAS active time | | tRAS | 40 | 100K | 42 | 100K | 45 | 100K | ns | |
| /RAS precharge time | | tRP | 14 | - | 18 | - | 20 | - | ns | |
| /RAS to /RAS bank active delay | | tRRD | 10 | - | 12 | - | 14 | - | ns | |
| /CAS to /CAS delay | | tCCD | 1 | - | 1 | - | 1 | - | CLK | |
| Data – out hold time | | tOH | 1.5 | - | 2 | - | 2.5 | - | ns | |
| Data – input setup time | | tDS | 1.5 | - | 1.5 | - | 1.5 | - | ns | 1 |
| Data – input hold time | | tDH | 1 | - | 1 | - | 1 | - | ns | 1 |
| Address setup time | | tAS | 1.5 | - | 1.5 | - | 1.5 | - | ns | 1 |
| Address hold time | | tAH | 1 | - | 1 | - | 1 | - | ns | 1 |
| Power down exit time | | tPDE | 5 | - | 5 | - | 5 | - | CLK | |
| Refresh time | | tREF | | 64 | | 64 | | 64 | ms | |

**Note :** 1. Assume tR / tF (input rise and fall time) is 1 ns.

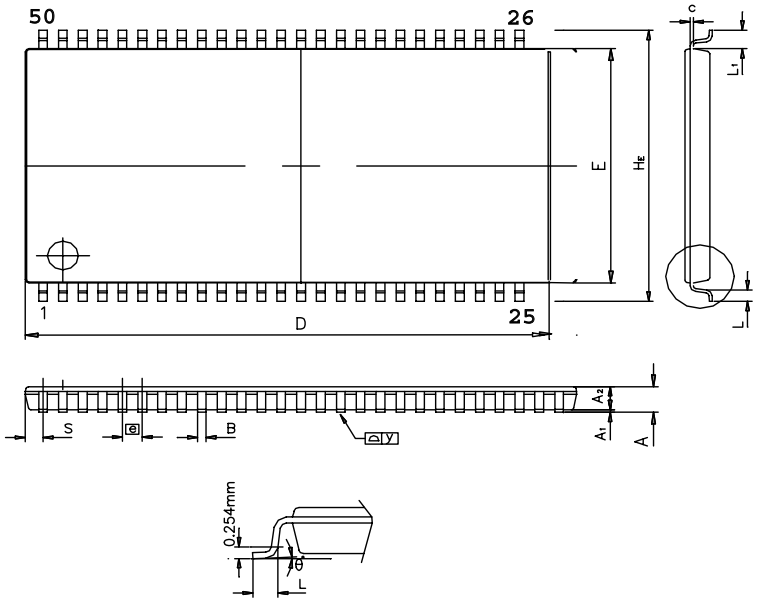
2. Access times to be measured with input signals of 1v / ns edge rate.

3.A new command can be given tRRC after self refresh exit.

## Command Truth-Table

| Command | | CKEn-1 | CKEn | /CS | /RAS | /CAS | /WE | A10 | A9-A0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Register Set | | H | X | L | L | L | L | X | V |
| No Operation | | H | X | L | H | H | H | X | X |
| Bank Active | | H | X | L | L | H | H | V | |
| Read | | H | X | L | H | L | H | L | V |
| Read with Auto Precharge | | | | | | | | H | |
| Write | | H | X | L | H | L | L | L | V |
| Write with Auto Precharge | | | | | | | | H | |
| Precharge All Bank | | H | X | L | L | H | L | H | X |
| Precharge select Bank | | | | | | | | L | X |
| Burst Stop | | H | X | L | H | H | L | X | |
| DQM | | H | X | | | | | X | |
| Self Refresh | Entry | H | L | L | L | L | H | X | |
| | Exit | L | H | H | X | X | X | | |
| | | | | L | H | H | H | | |
| Precharge Power down | Entry | H | L | X | | | | X | |
| | Exit | L | H | X | | | | | |
| Clock Suspend | Entry | H | L | X | | | | X | |
| | Exit | L | L | X | | | | | |

## Package Information




| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| B | 0.30 | | 0.45 | 0.012 | | 0.018 |
| c | 0.12 | | 0.21 | 0.005 | | 0.008 |
| D | 21.08 BSC | | | 0.830 BSC | | |
| $H_E$ | 11.56 | 11.76 | 11.96 | 0.460 | 0.463 | 0.471 |
| E | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 0.80 BSC | | | 0.0315 | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.80 REF | | | 0.031 REF | | |
| S | 0.71 REF | | | 0.028 REF | | |
| θ | 0 ° | - | 5 ° | 0 ° | - | 5 ° |

400mil 50pin TSOP II Package